Lecture 4 – Monolithic Microwave Integrated Circuits

- **Review of Semiconductor Physics**

  Semiconductor materials, heterojunction and HEMT.

- **MMIC Manufacturing Technology**

  MMIC manufacturing process, foundry service.

- **MMIC Design Technology**

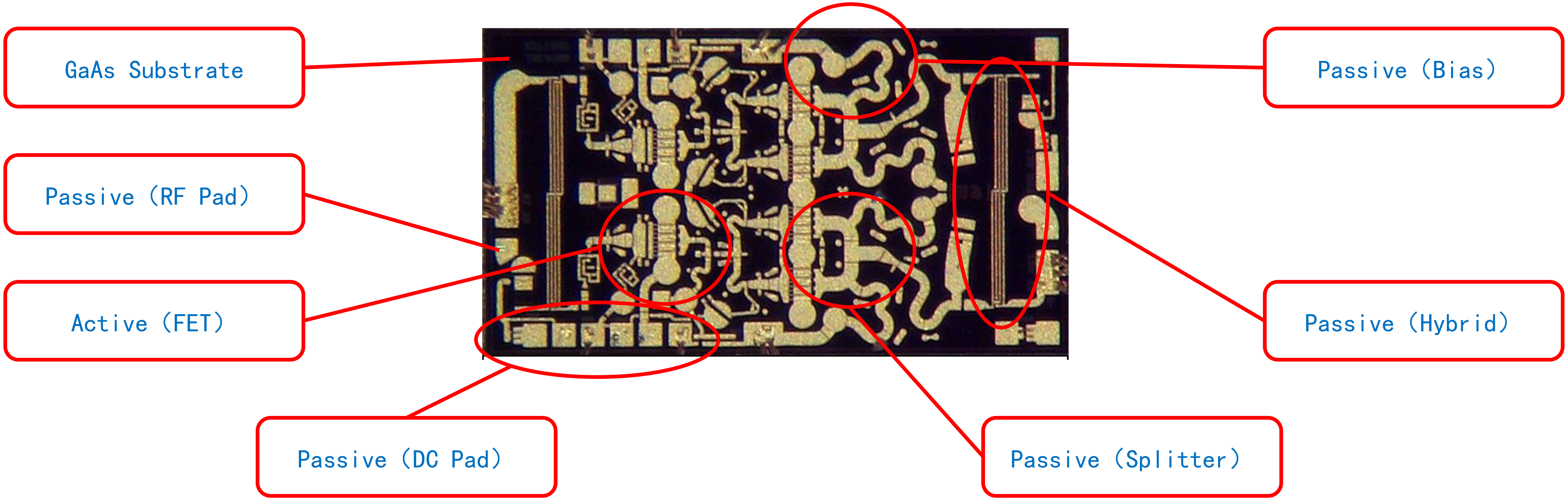
  Modeling and Process design kit, simulation and design software.

- **MMIC Measurement**

  Probe station, probes, calibration, automatic measurement.

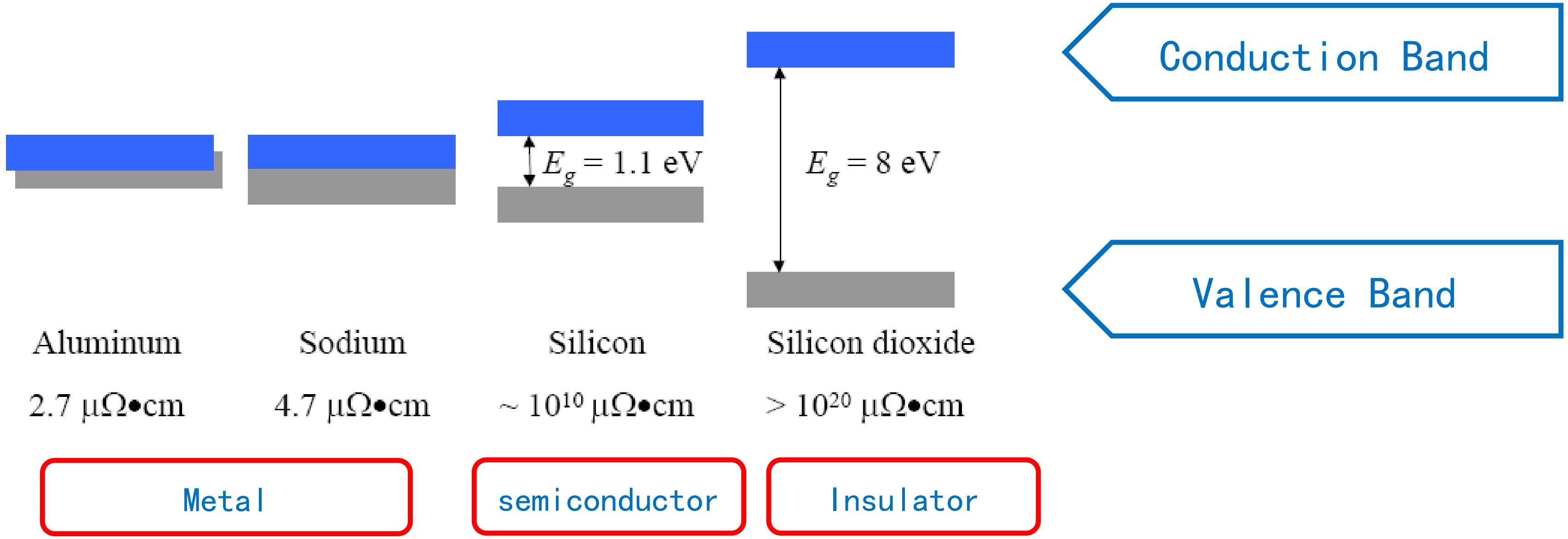
Monolithic Microwave Integrated Circuits (MMIC)

MMIC is a type of microwave integrated circuit that integrates active and passive circuits in single semiconductor substrate. These devices typically perform functions such as microwave mixing, power amplification, low-noise amplification, and high-frequency switching.



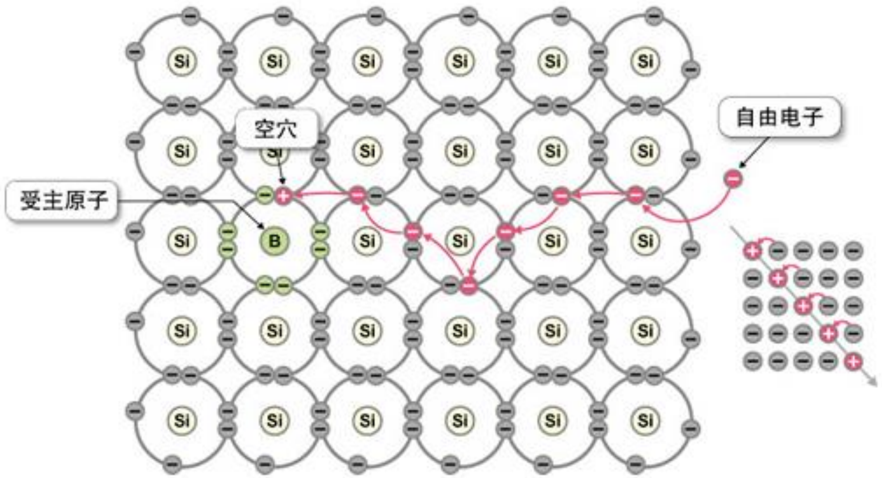
Semiconductor and variable conductivity

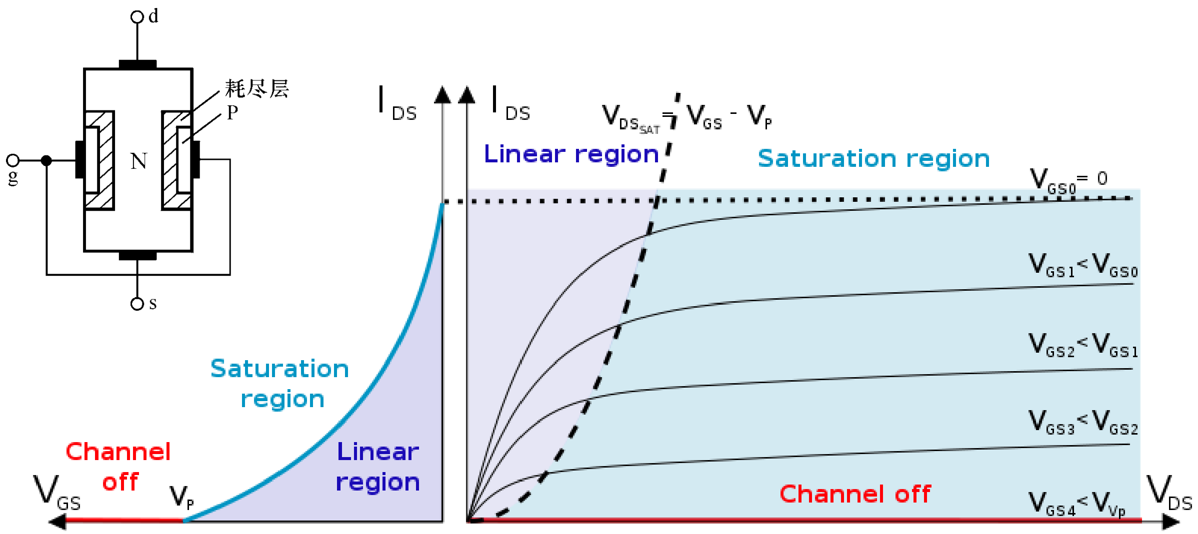
Semiconductors in their natural state are poor conductors because a current requires the flow of electrons, and semiconductors have their valence bands filled, preventing the entry flow of new electrons.



Semiconductor and variable conductivity

There are several developed techniques that allow semiconducting materials to behave like conducting materials, such as doping or gating.





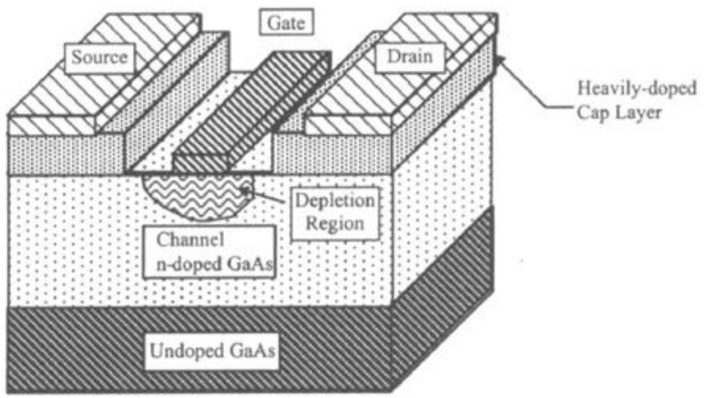
Semiconductor materials

	G1	G2		G3	
Parameters	Si	GaAs	InP	GaN	SiC
Bandgap (eV)	1.12	1.42	1.35	3.4	3.2
Breakdown (MV/cm)	0.38	0.42	0.5	3.3	3
Therm Cond (W/cm•k)	1.4	0.45	0.68	3	4.5
Sat Velocity (10^7cm/s)	0.7	2.1	2.3	2.1	0.2
Mobility (cm^2/vs)	1500	8500	5400	2000	1500
Dielectric Const	11.8	12.8	8	14	10
Working Temp (°C)	200	350	300	600	800
Rad Resistance (rad)	10^4	10^6	10^6	10^{10}	10^{10}

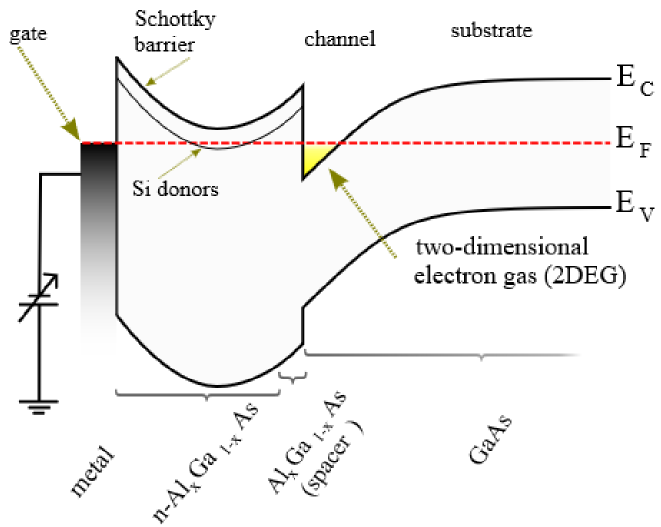
Heterojunction and HEMT

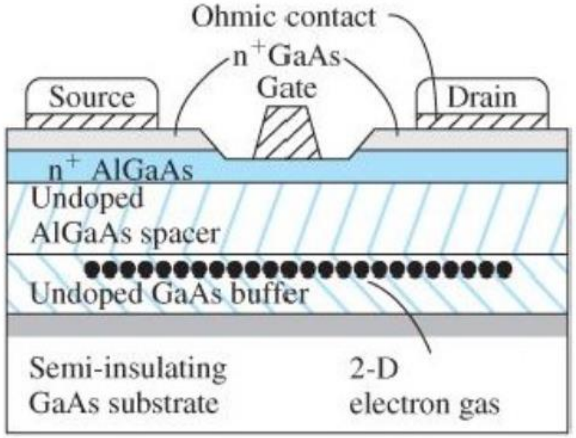
Heterojunctions occur when two differently doped semiconducting materials are joined together.

A High-electron-mobility transistor (HEMT) is a field-effect transistor incorporating a junction between two materials with different band gaps (i.e. a heterojunction) as the channel instead of a doped region (as is generally the case for MESFET).



MESFET



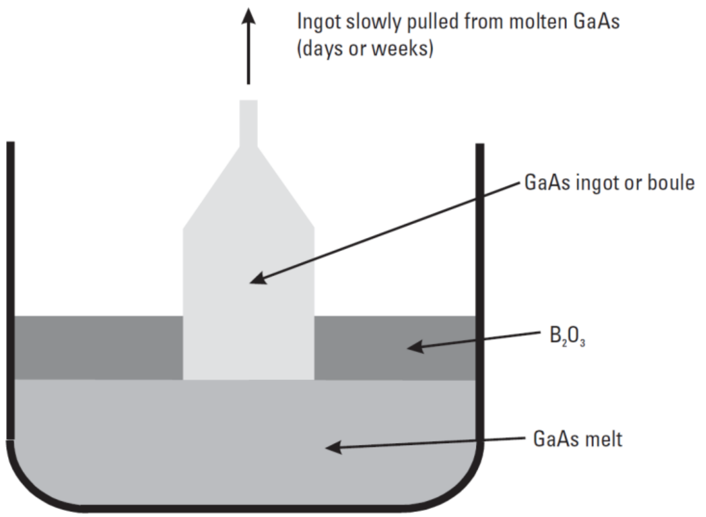


HEMT

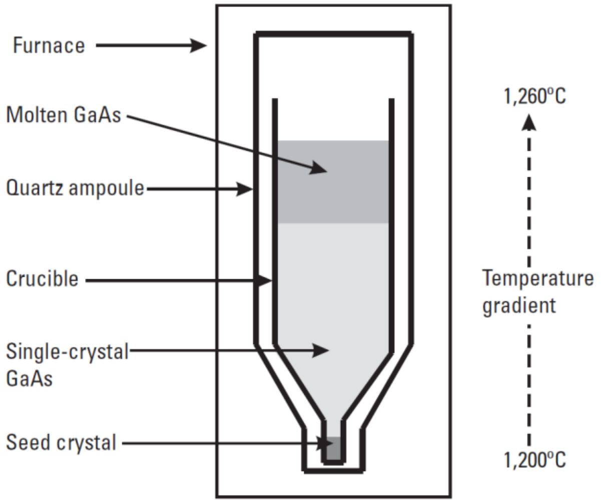
Substrate material growth

Single-crystal substrate growth techniques:

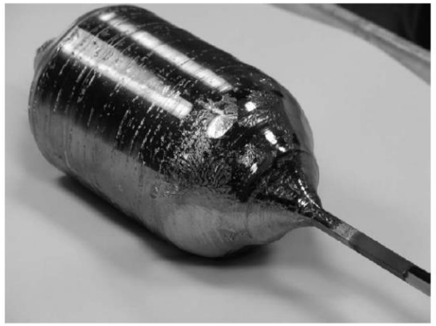
Liquid-Encapsulated Czochralski (LEC) and Vertical Gradient Freeze (VGF)

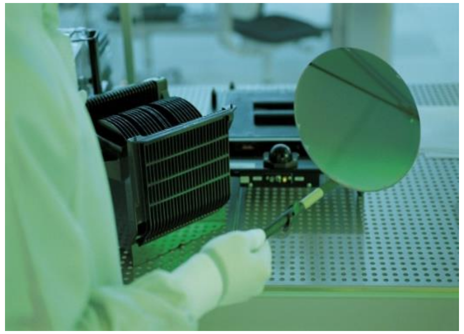


LEC



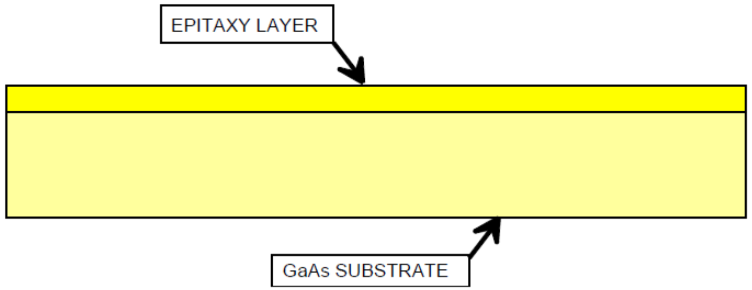
VGF

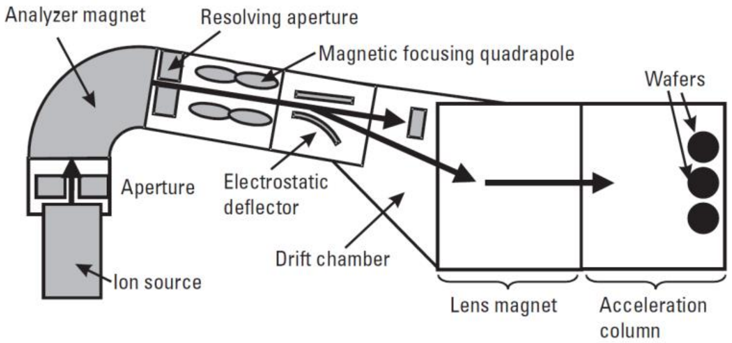


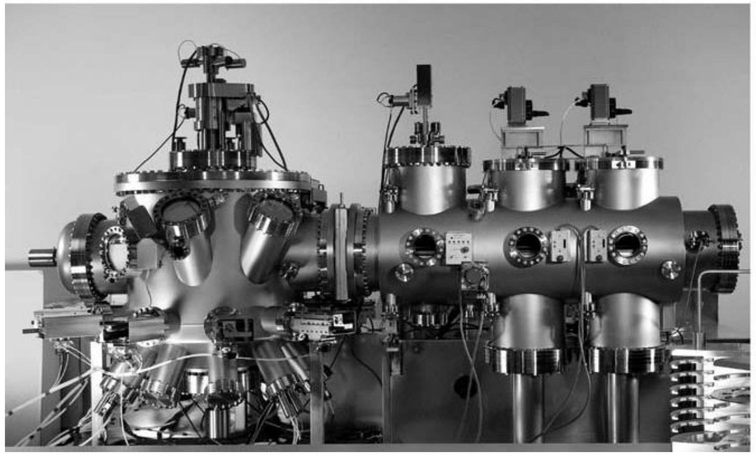


Creating an active layer

There are three ways to make the semiconductor conducting on the wafer surface:





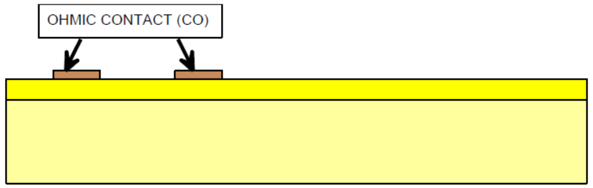


Ion implantation

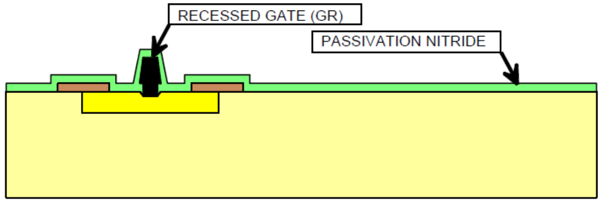
Molecular beam epitaxy (MBE)

Metal-organic chemical vapor deposition (MOCVD)

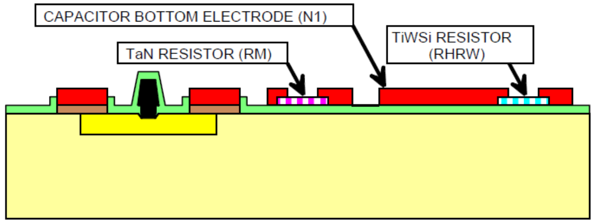
Photolithography



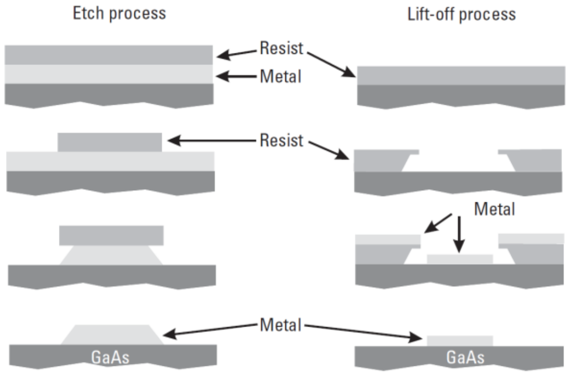
Ohmic Contact

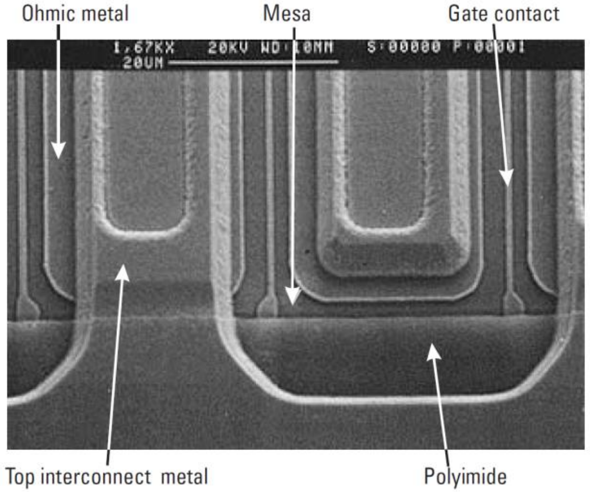


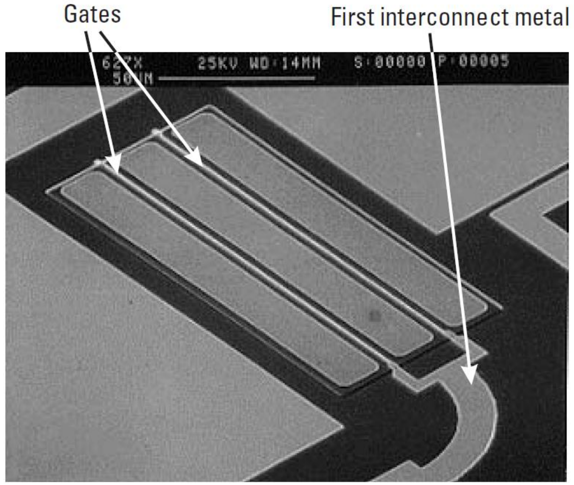
Gate Contact & Passivation



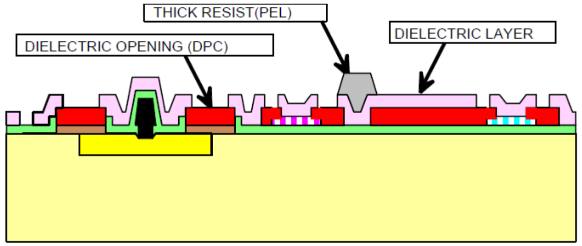
First & Resistive Metals

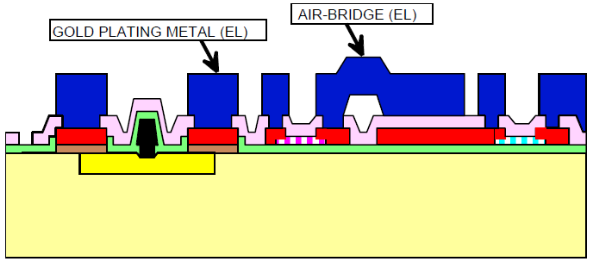


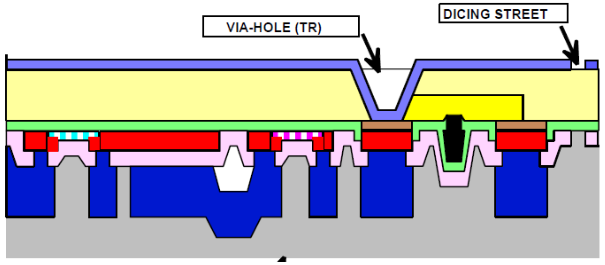




Photolithography



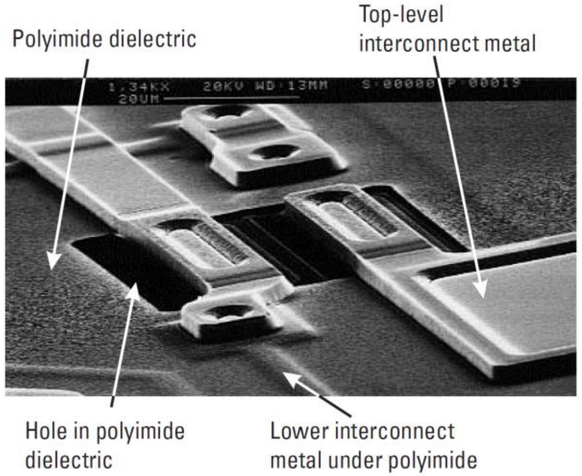


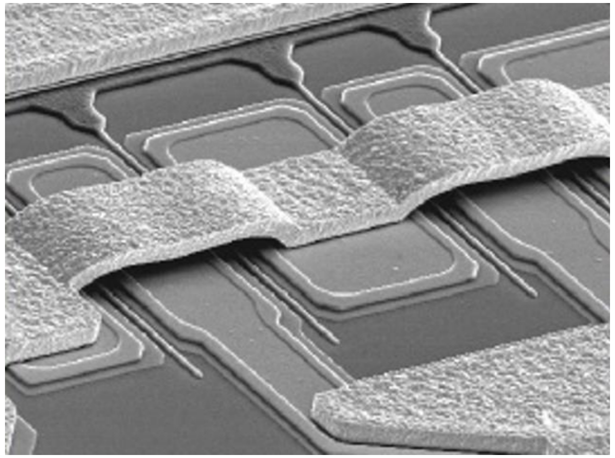


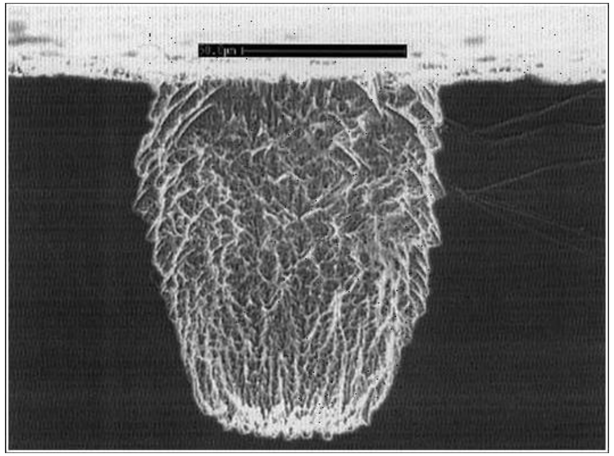
Dielectric Layers

Top Metal & Air Bridge

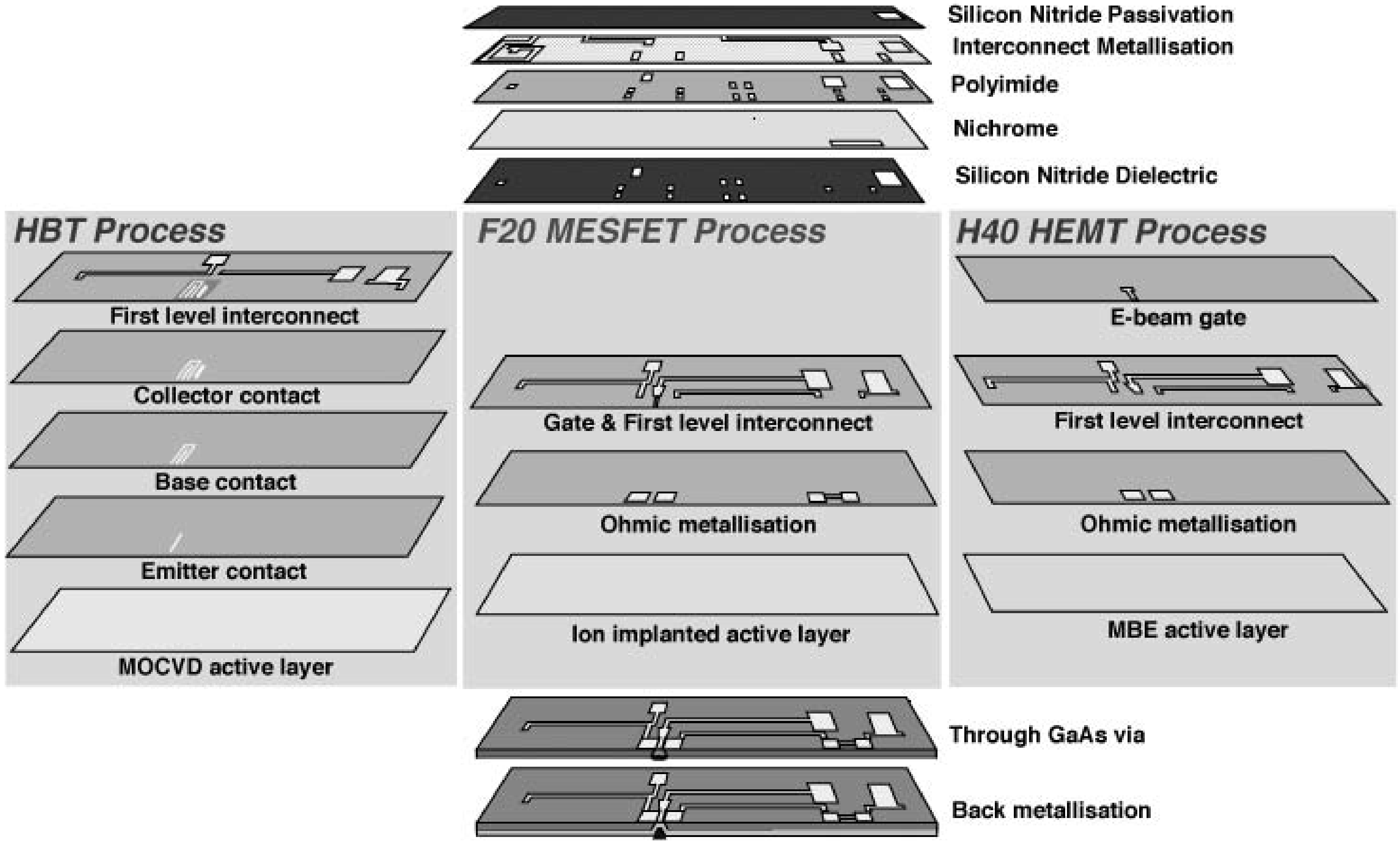
Thru-sub Via & Back Metal



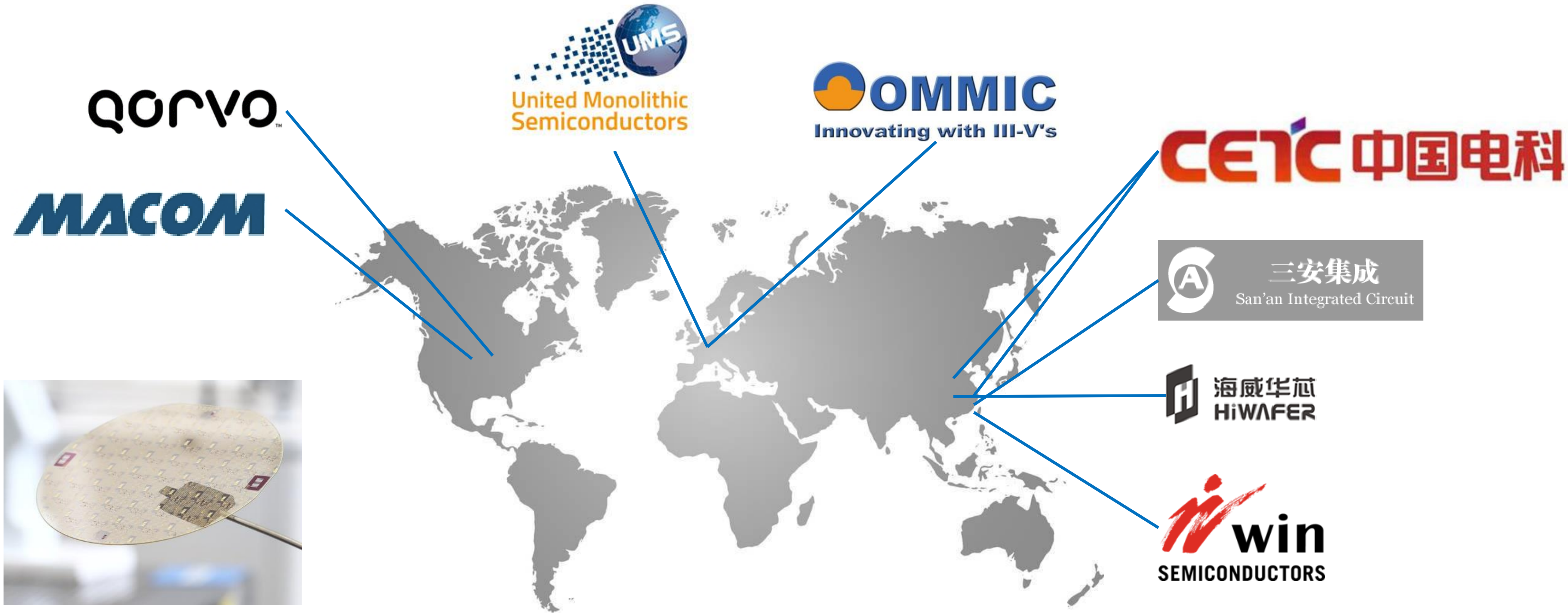




- **Typical MMIC process layers**

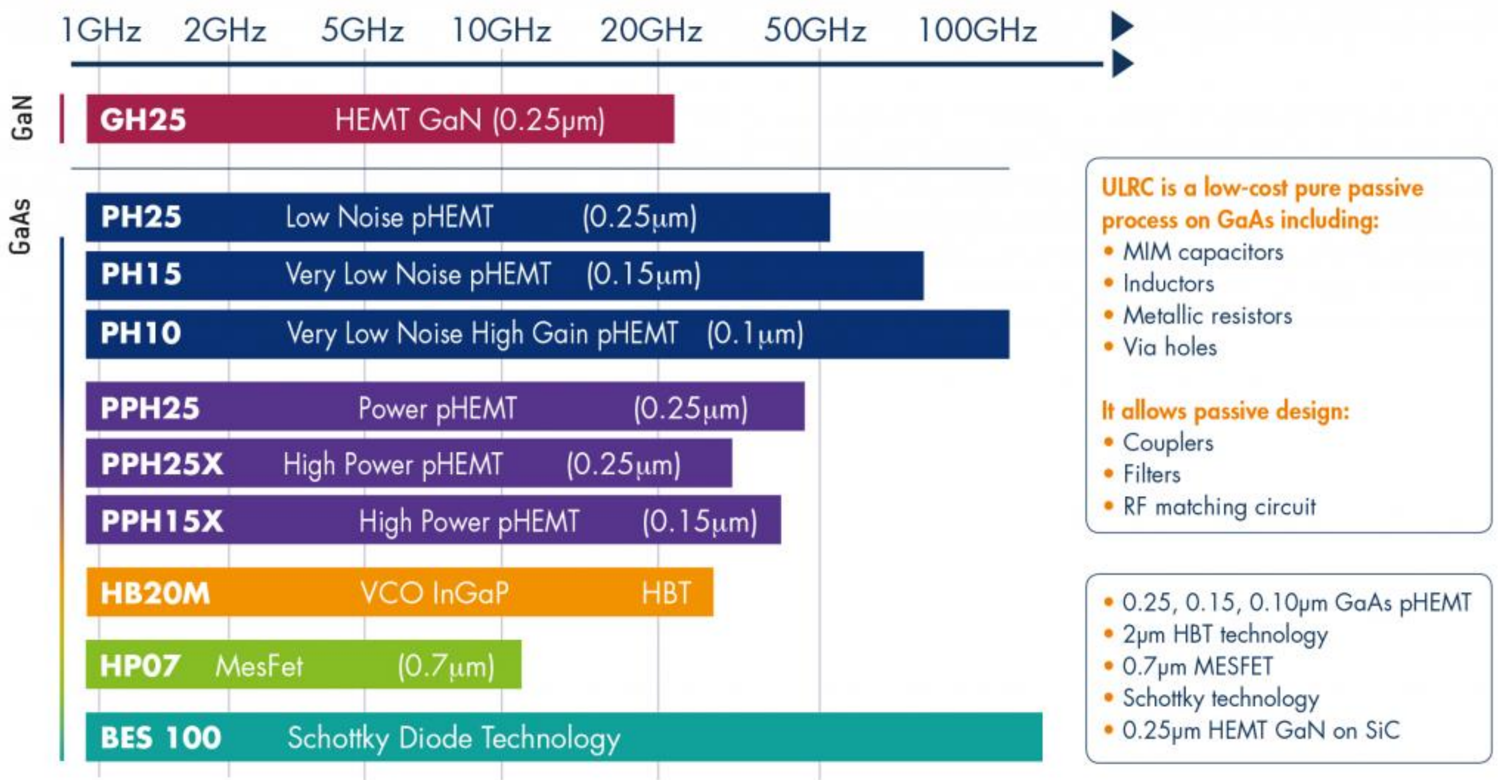


■ Foundry Services (GaAs/GaN)



Foundry Services (GaAs/GaN)

United Monolithic Semiconductors



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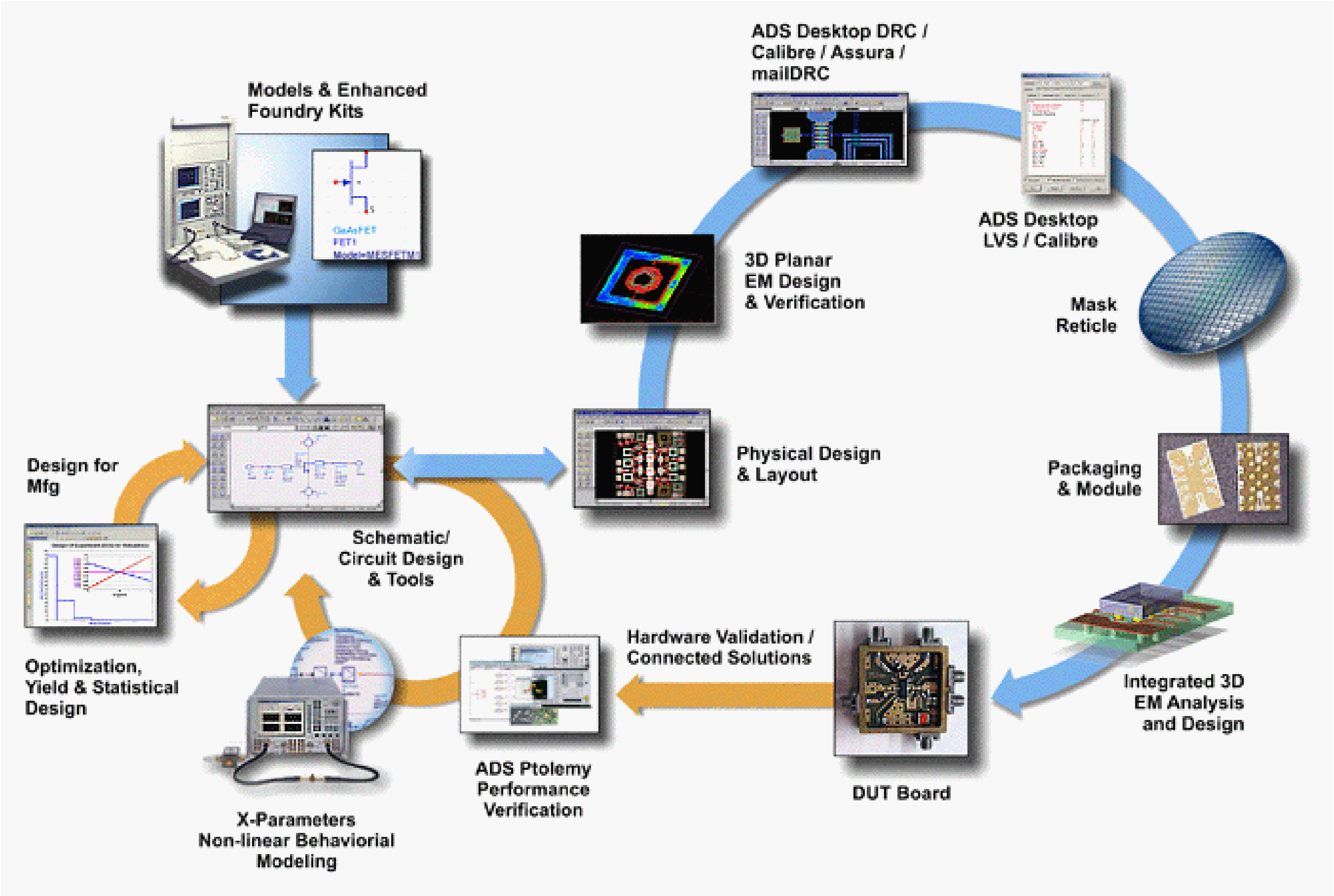
Foundry Services (GaAs/GaN)

United Monolithic Semiconductors

Process	GH25 GaN	PH25 Low Noise	PH15 Low Noise	PH10 Low Noise	PPH25 Power	PPH25X High Power	PPH15X High Power	HB20M VCO	HP07	BES
Active device	HEMT	pHEMT	pHEMT	pHEMT	pHEMT	pHEMT	pHEMT	HBT	MESFET	Schottky
Power Density	4.5W/mm	250mW/mm	300mW/mm	250mW/mm	700mW/mm	900mW/mm	800mW/mm	2W/mm	400mW/mm	-
Gate Length	0.25µm	0.25µm	0.15µm	0.1µm	0.25µm	0.25 µm	0.15µm	2µm Emitter width	0.7µm	1µm
Ids (gm max) Ids sat/Ic	750mA/mm 1000mA/mm	200mA/mm 500mA/mm	220mA/mm 550mA/mm	280mA/mm	200mA/mm 500mA/mm	170mA/mm 450mA/mm	350mA/mm 575mA/mm	0.3mA/µm²	300mA/mm 450mA/mm	-
V_{BDS} / V_{BCE}	>100V	> 6V	> 4.5V	> 5V	> 12V	> 18V	> 12V	> 14V	> 14V	< -5V (Anode/ Cathode
Cut off freq.	30GHz	90GHz	110GHz	130GHz	50GHz	45GHz	70GHz	30GHz	15GHz	3THz
Vpinch	-3.4V	- 0.8V	- 0.7V	-0.45V	- 0.9V	- 0.9V	- 0.95V	-	- 4.0V	-
Gm max / β	300mS/mm	560mS/mm	640mS/mm	750mS/mm	450mS/mm	400mS/mm	480mS/mm	60	110mS/mm	-
Noise / Gain	1.8dB/11dB @15GHz	0.6dB / 13dB @10GHz 2dB / 8dB @40GHz	0.5dB / 14dB @10GHz 1.9dB / 6dB @60GHz	2.3dB / 4.5dB @70GHz	0.6dB / 12dB @10GHz	-	1.8dB / 6dB @40GHz	-	-	-

MMIC design procedure



MMIC design software

Cadence

Layout, LVS and DRC Check

Circuit-Level Simulation

ADS

Circuit-Level and EM Simulation

Layout, DRC Check

Ansoft HFSS

EM-Level Simulation

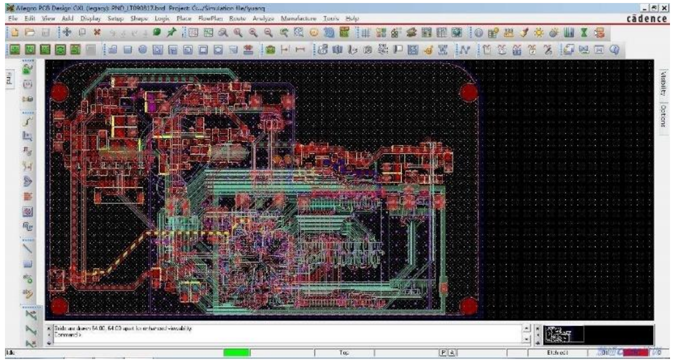
AWR Microwave Office

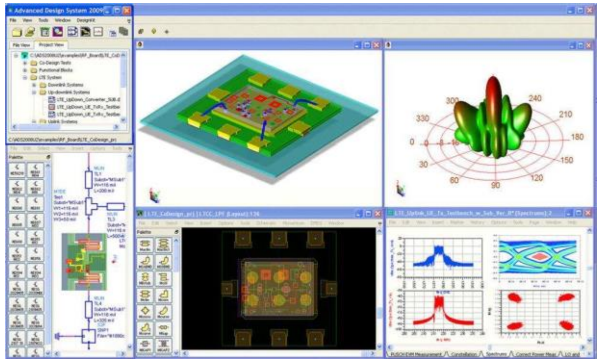
Circuit-Level and EM Simulation

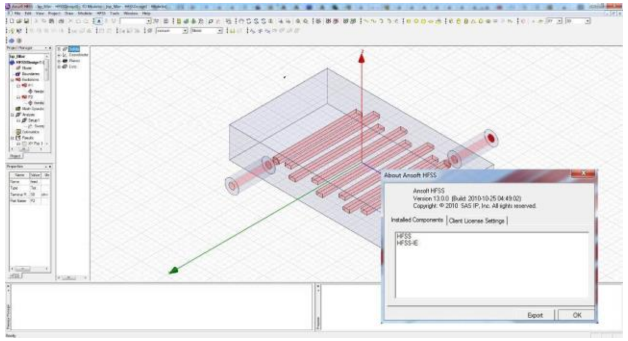
Layout, DRC Check

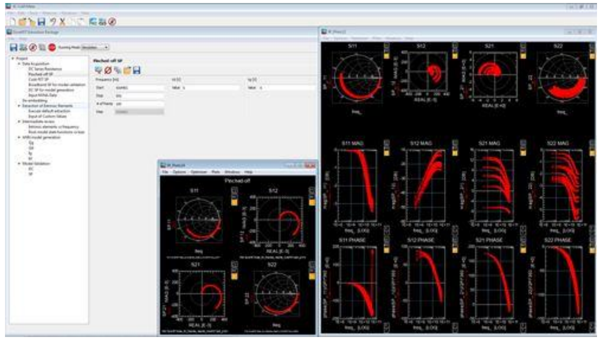
IC-CAP

Modelling Software



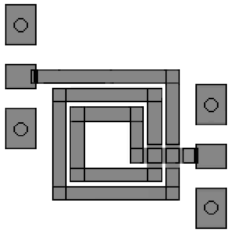


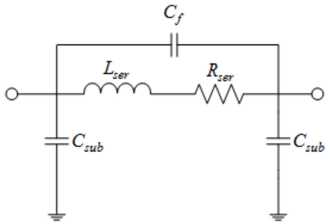


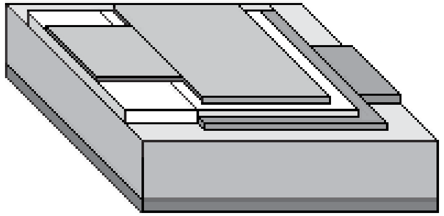


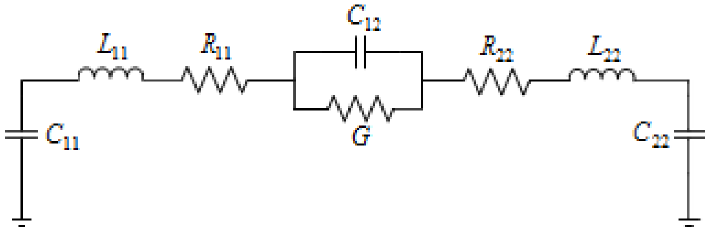
Modeling and Process Design Kit (PDK)

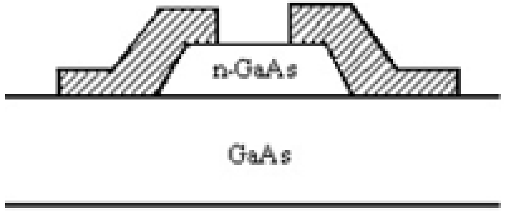
Passive device modeling (linear)

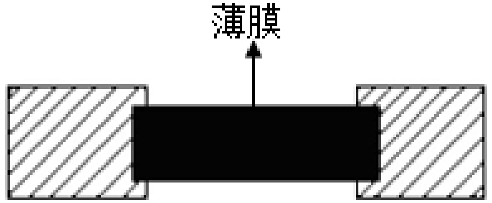


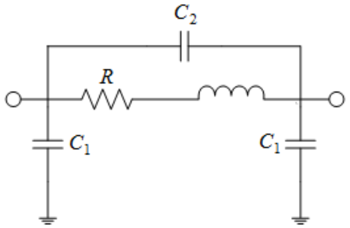


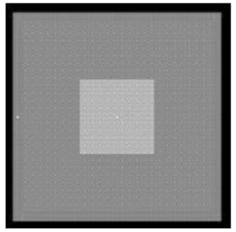


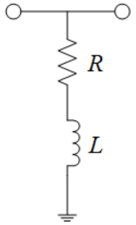






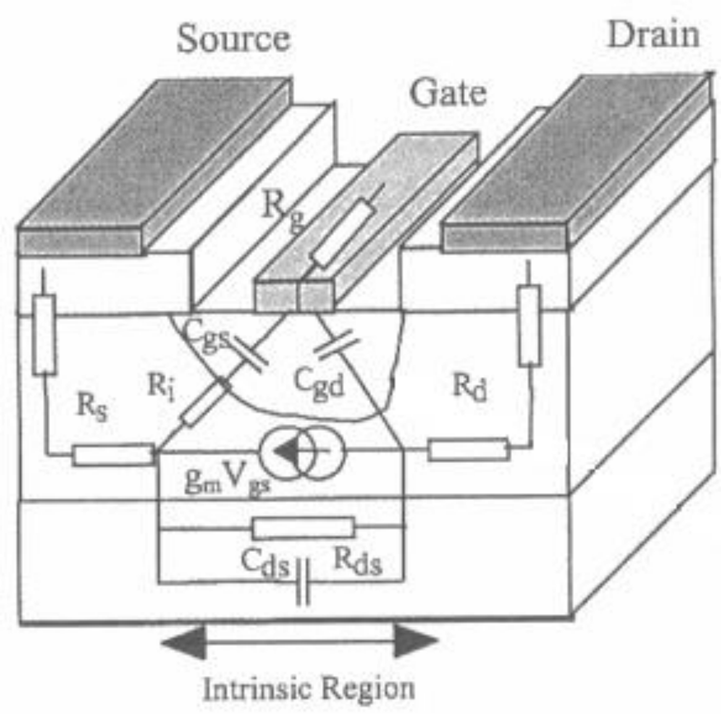


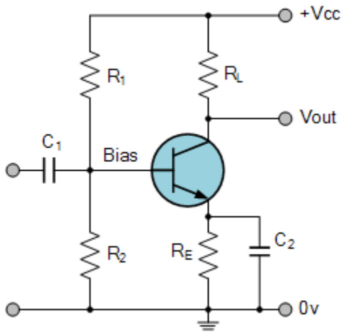


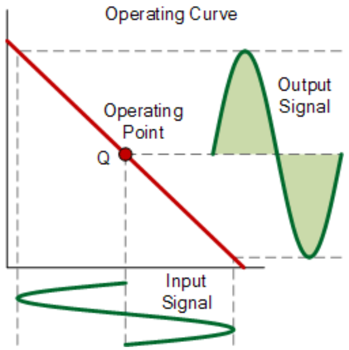


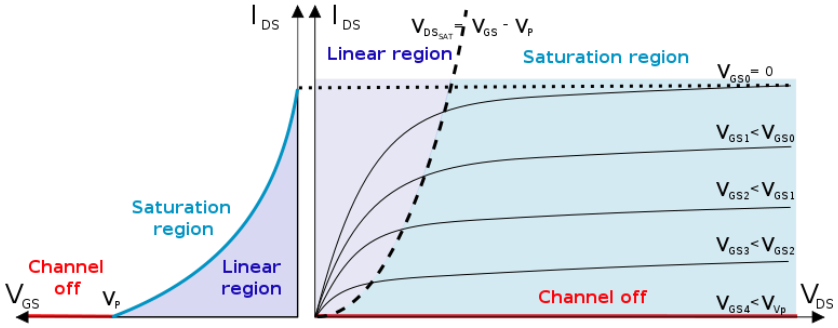
Modeling and Process Design Kit (PDK)

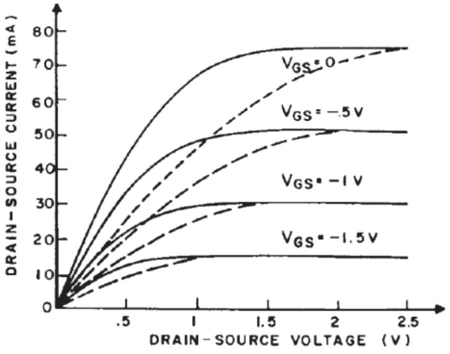
Active device modeling (non-linear)





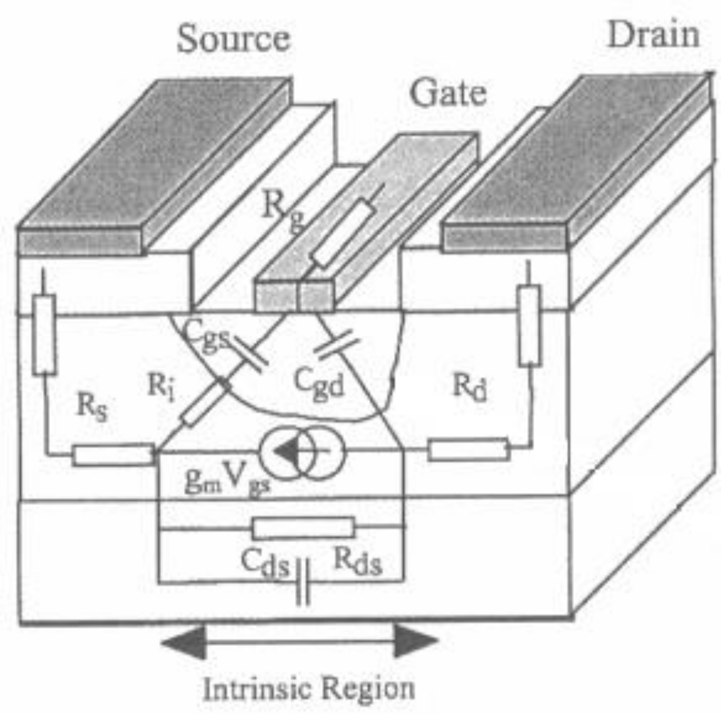






Modeling and Process Design Kit (PDK)

Modeling techniques

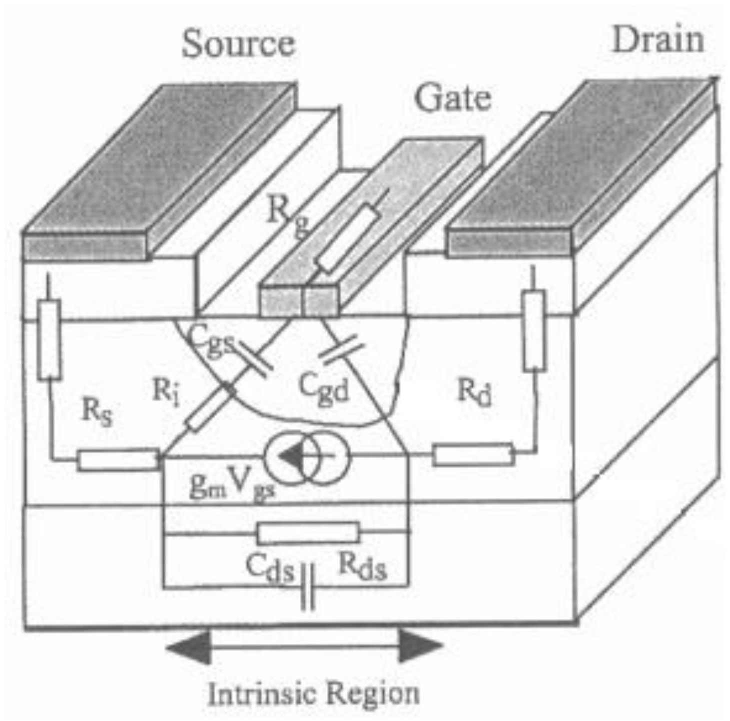


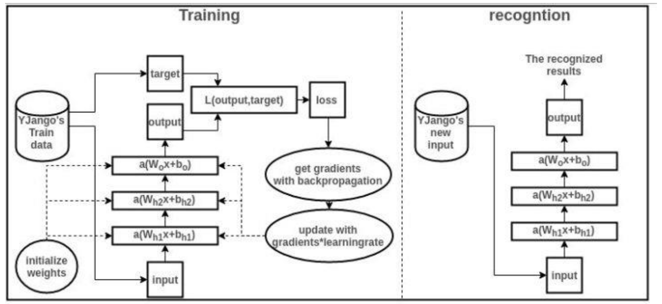
- Analytical Model
- Numerical Model
- Empirical Model

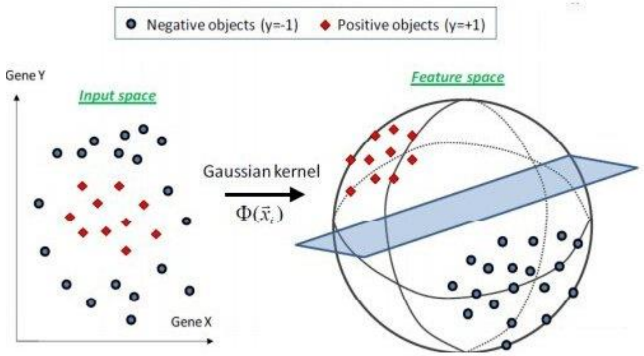
Time	Model	Remarkable Contribution
1980 Curtice	Curtice Model	First Empirical Model
1987 Staz	Staz Model	2D Capacitance Model
1990 McCamant et al.	TOM	Negative DC Conductance
1991 Root	Root Model	First Table-based Model
1992 Angelov	Chalmers Model	Continuity to High Orders
1993 EESOF	EEFET/EEHEMT	RF Current Added
1997 Parker, Cojacoru	Parker Model/Corbra Model	Continuity to High Orders
1996-1997 Rolain, Wei	Black-box Models	General Device Modeling
1997- Wei	Enhanced TOM/AODM Models	Dispersion Handled Better
1997- Schreurs	Black-box Modeling	Time-domain
1999-Smiths	TOM3	

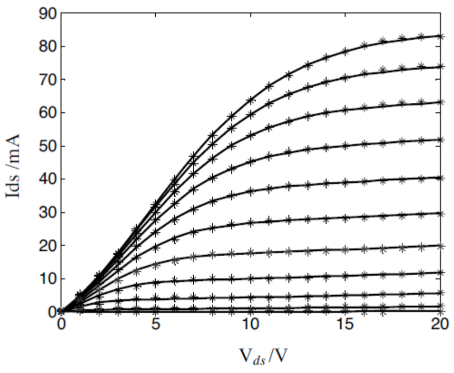
Modeling and Process Design Kit (PDK)

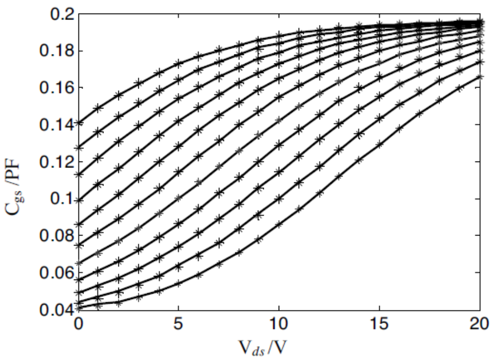
Modeling techniques – Empirical model





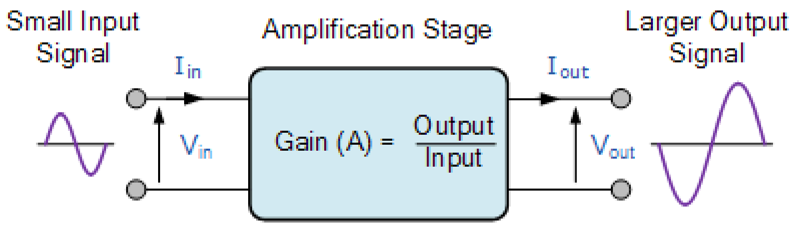




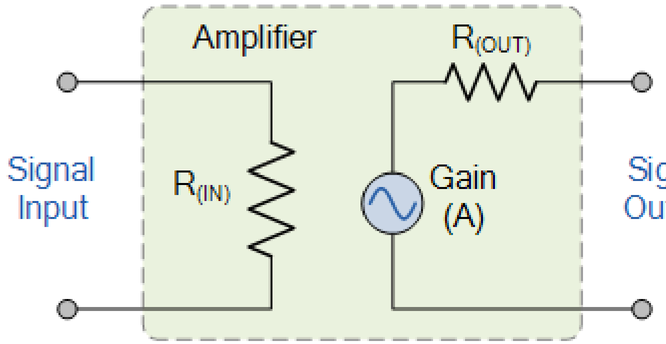


■ Circuit Design (Amplifier)

Amplifier is the generic term used to describe a circuit which increases its input signal, but not all amplifiers are the same as they are classified according to their circuit configurations and methods of operation.

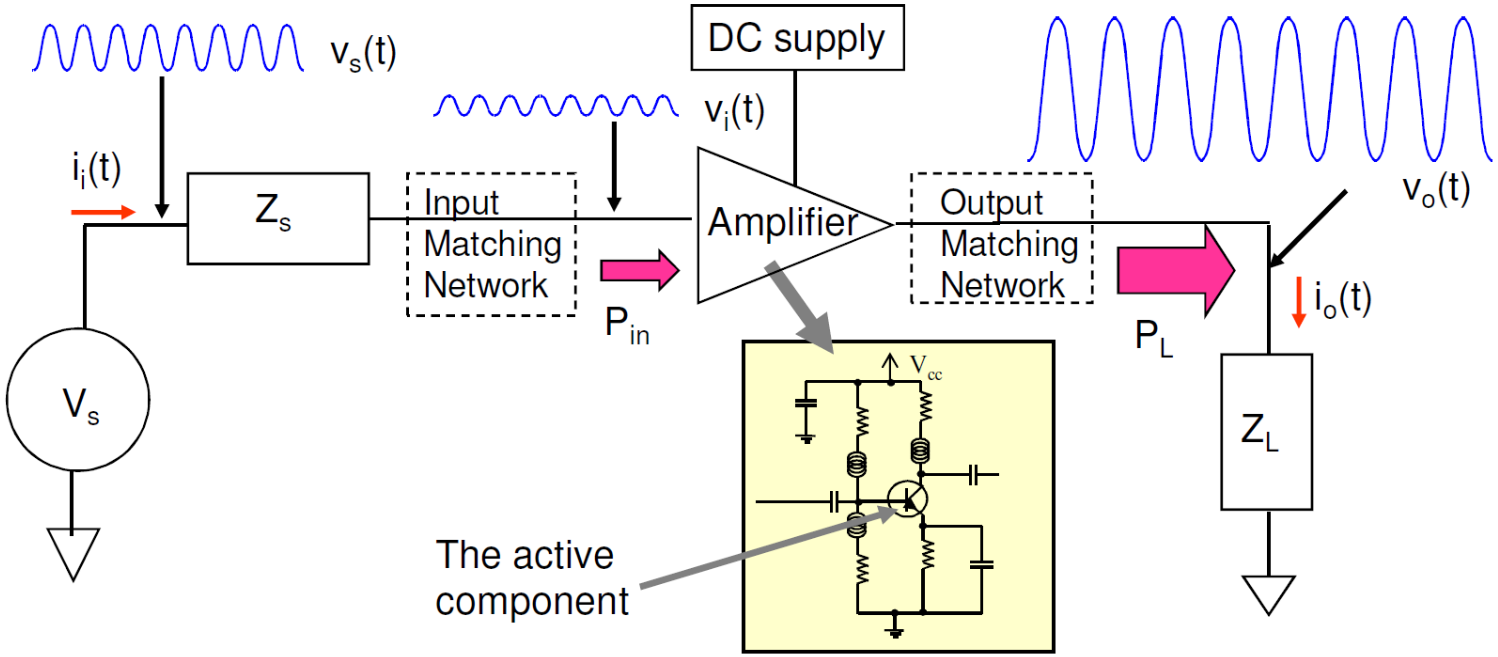


The difference between the input and output signals is known as the Gain of the amplifier and is basically a measure of how much an amplifier "amplifies" the input signal.



Circuit Design (Amplifier)

A general amplifier block diagram:



Input and output voltage relation of the amplifier can be modeled simply as:

$$v_o(t) = a_1 v_i(t) + a_2 v_i^2(t) + a_3 v_i^3(t) + H.O.T.$$

Circuit Design (Amplifier)

Amplifier Classification

According to signal level:

– Small-signal Amplifier.

– Power/Large-signal Amplifier.

According to D.C. biasing scheme of the active component:

– Class A.

– Class B.

– Class AB.

– Class C.

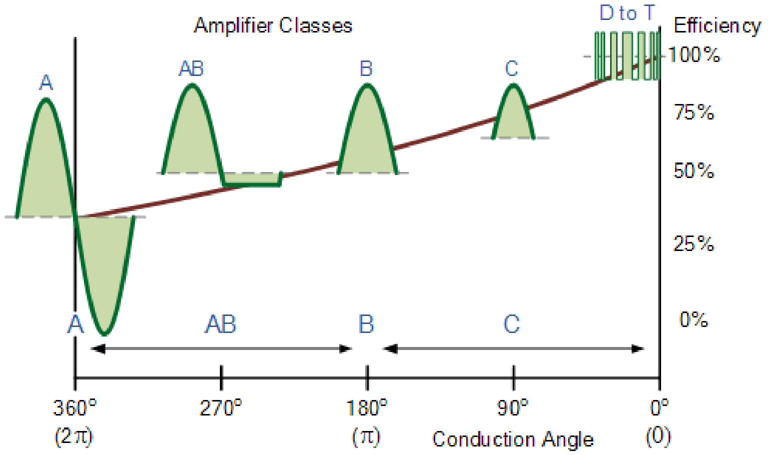
– Class D.

– Class E.

– Class F.

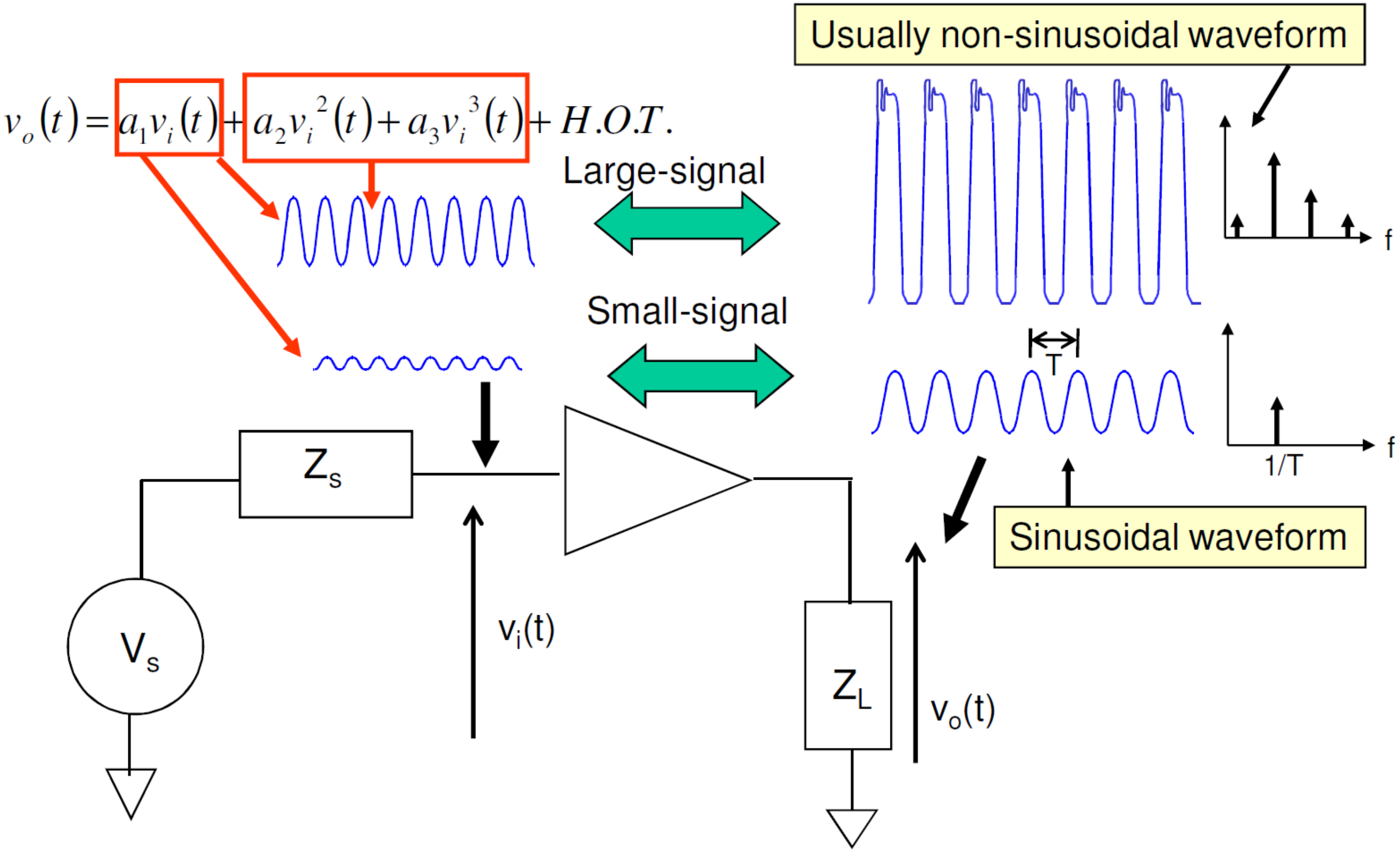
…

Switch-Mode Amplifiers



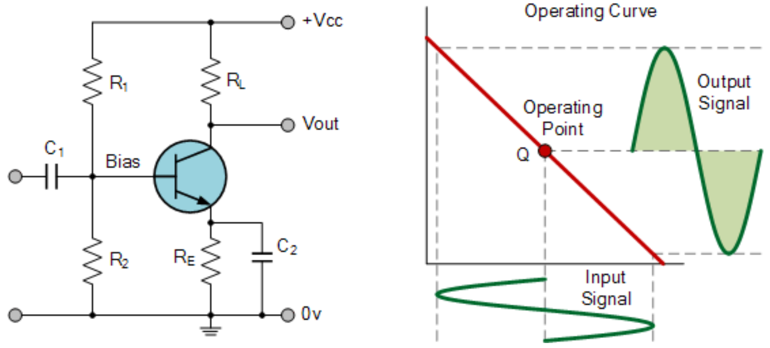
Circuit Design (Amplifier)

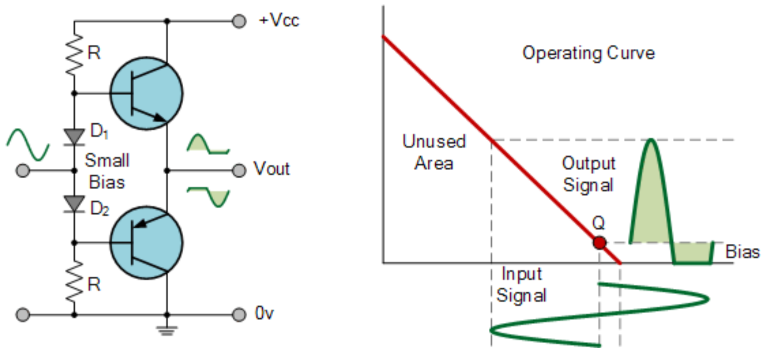
Amplifier Classification (Small Signal v.s. Large Signal Operation)

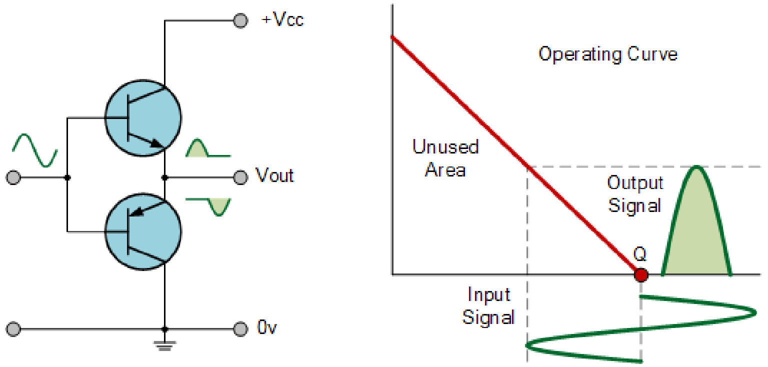


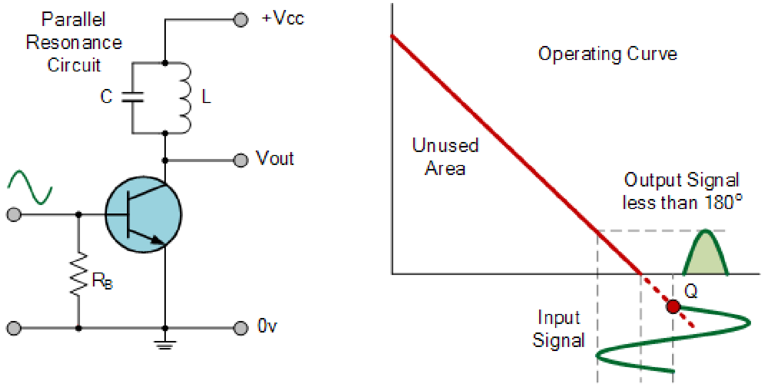
Circuit Design (Amplifier)

Amplifier Classification (according to D.C. biasing scheme of the active component)









Circuit Design (Amplifier)

Typical Microwave Amplifier Characteristics

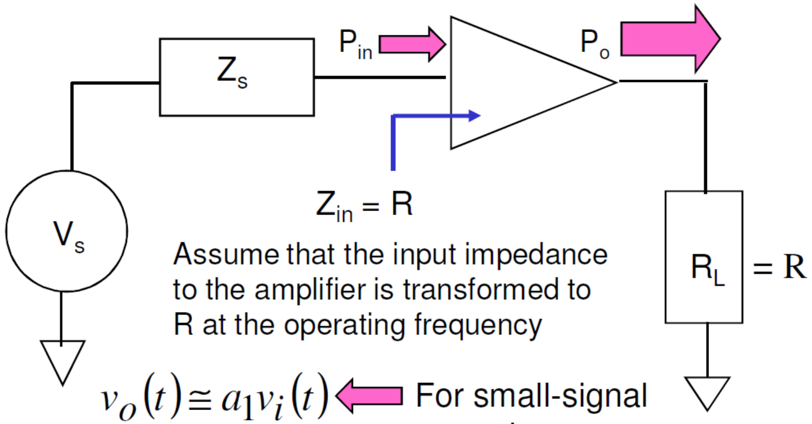
- 1. Power Gain.
- 2. Bandwidth (operating frequency range).
- 3. Noise Figure.
- 4. Phase response.
- 5. Gain compression.
- 6. Dynamic range.
- 7. Harmonic distortion.
- 8. Intermodulation distortion.
- 9. Third order intercept point (TOI).

Important to small-signal amplifier

Important parameters of large-signal amplifier (Related to Linearity)

Circuit Design (Amplifier)

Power Gain & Bandwidth



Assume that the input impedance to the amplifier is transformed to R at the operating frequency

$$G = 10\log_{10}\left(\frac{\text{Output Power}}{\text{Input Power}}\right)\ \text{dB}$$

$v_o(t) \cong a_1 v_i(t)$ ← For small-signal operation

$$\frac{1}{2R}{v_o}^2 \cong {a_1}^2 \frac{1}{2R}{v_i}^2$$

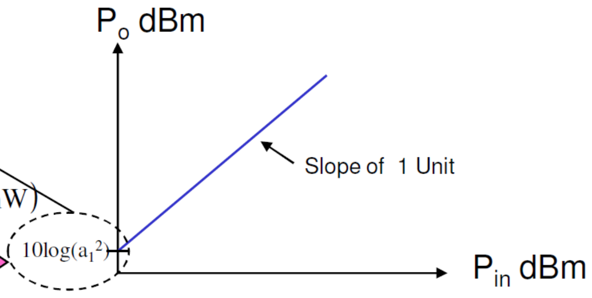
$$\Rightarrow P_o \cong a_1^2 P_{in}$$

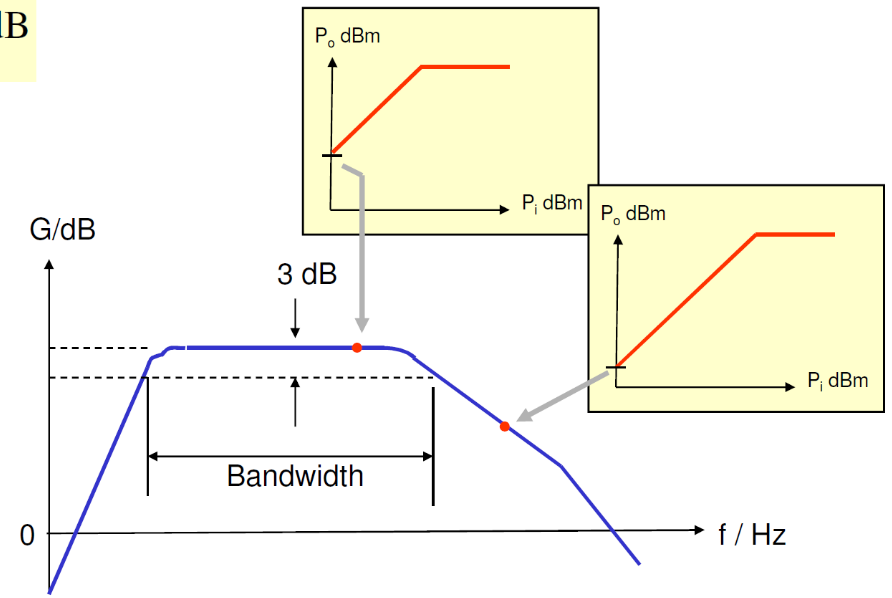
$$\Rightarrow P_o/1\text{mW} \cong a_1^2 (P_{in}/1\text{mW})$$

Power gain

$$\Rightarrow 10\cdot\log(P_o/1\text{mW}) \cong 10\cdot\log(a_1^2) + 10\cdot\log(P_{in}/1\text{mW})$$

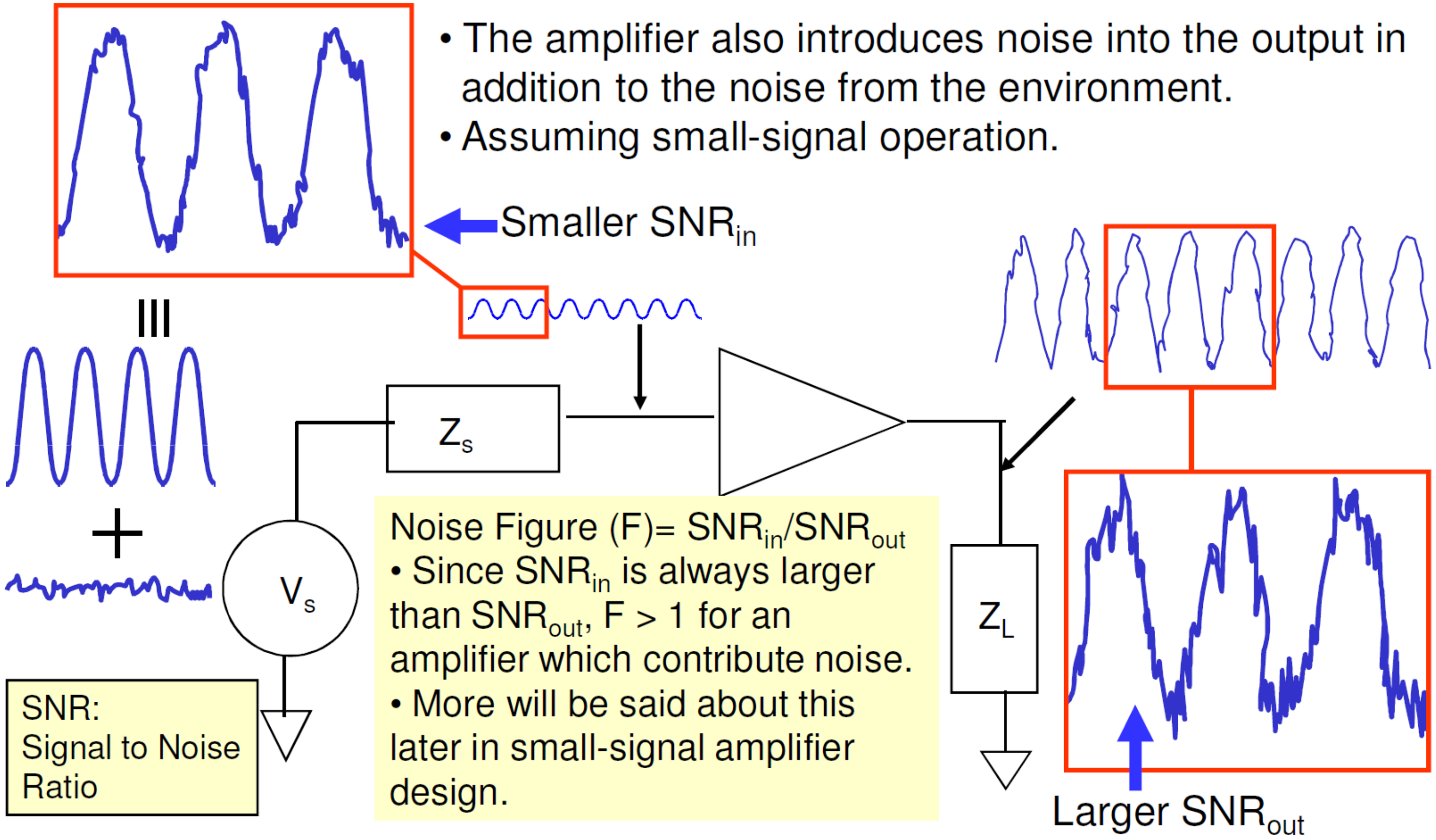
$$\Rightarrow \boxed{P_o dBm \cong 10\cdot\log(a_1^2) + P_{in} dBm}$$





Circuit Design (Amplifier)

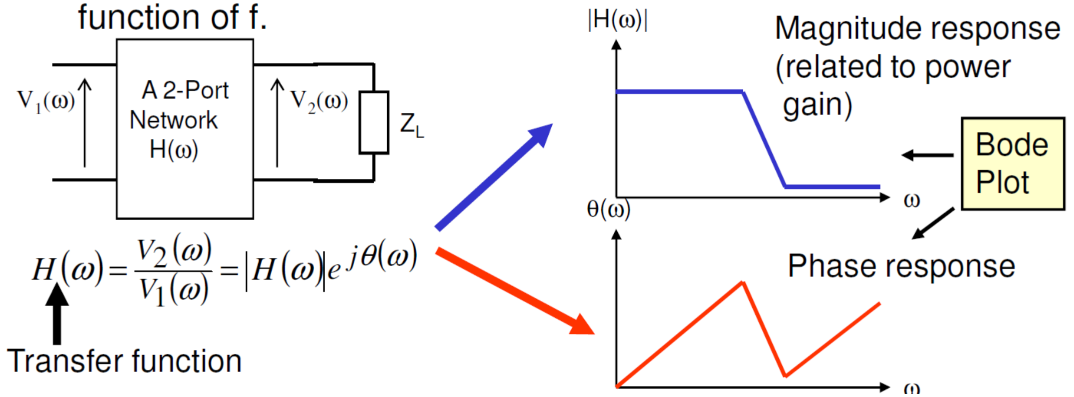
Noise Figure



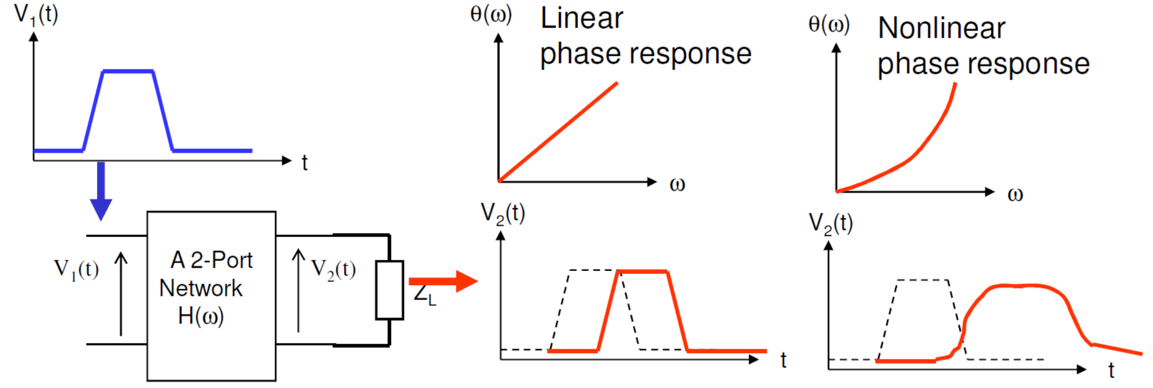
Circuit Design (Amplifier)

Phase Response

- Phase consideration is important for amplifier working with wideband signals.
- For a signal to be amplified with no distortion, 2 requirements are needed (from linear systems theory).
  - 1. The magnitude of the power gain transfer function must be a constant with respect to frequency f.
  - 2. The phase of the power gain transfer function must be a linear function of f.

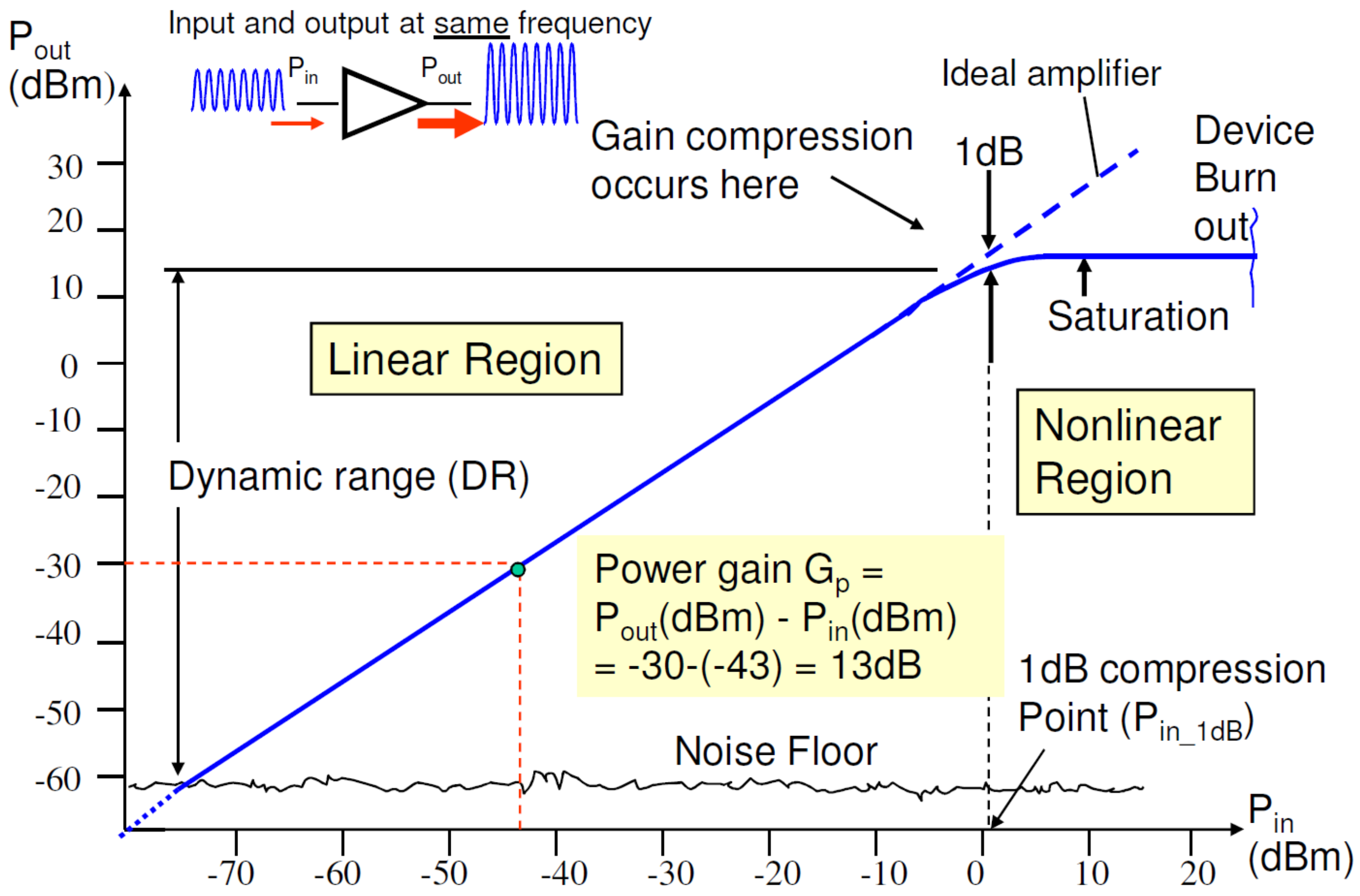


- A linear phase produces a constant time delay for all signal frequencies, and a nonlinear phase shift produces different time delay to different frequencies.
- Property (1) means that all frequency components will be amplified by similar amount, property (2) implies that all frequency components will be delayed by similar amount.



Circuit Design (Amplifier)

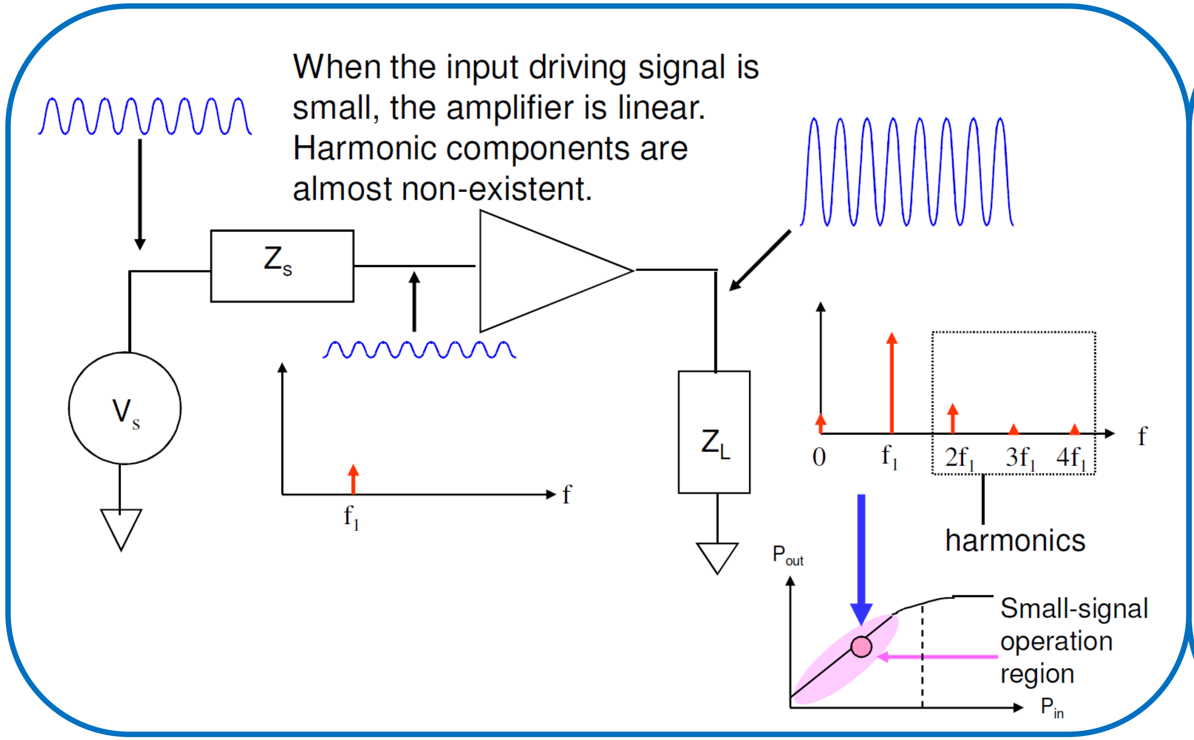
Dynamic Range and Gain Compression

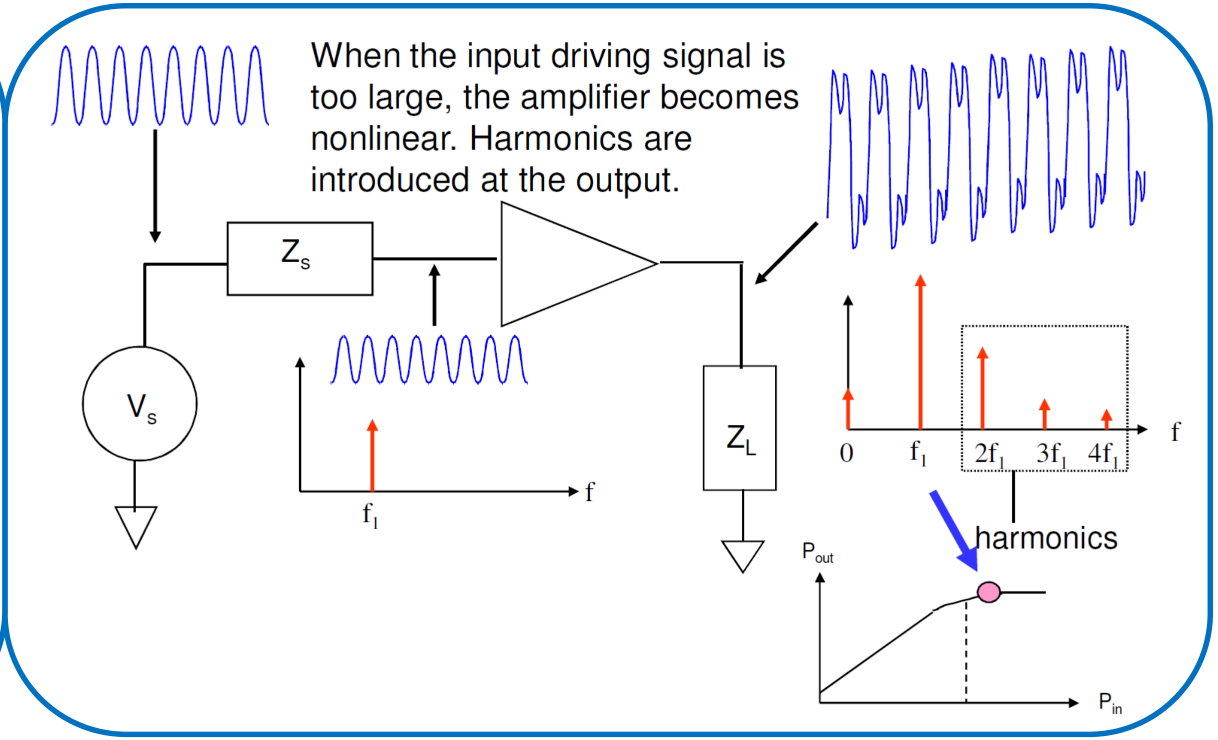


Circuit Design (Amplifier)

Harmonic Distortion

Harmonics generation reduces the gain of the amplifier, as some of the output power at the fundamental frequency is shifted to higher harmonics. This result in gain compression.

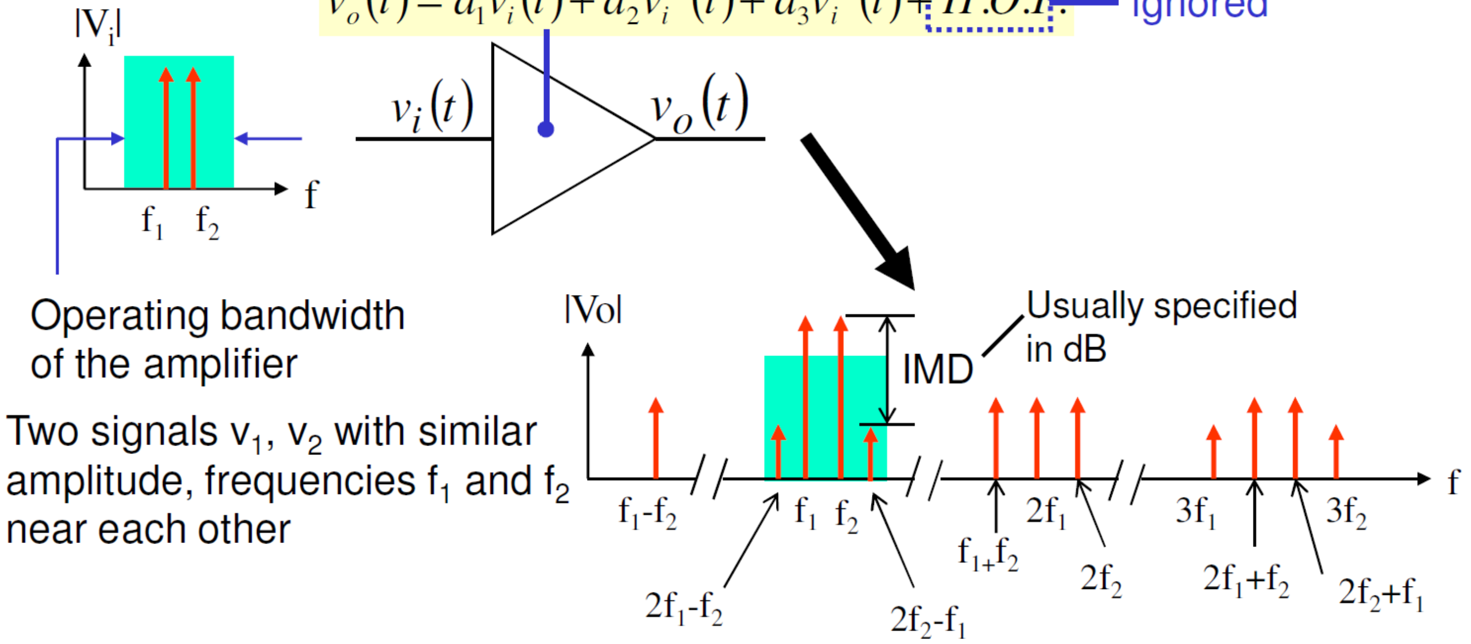




Circuit Design (Amplifier)

Intermodulation Distortion (IMD)

$$v_o(t) = a_1 v_i(t) + a_2 v_i^2(t) + a_3 v_i^3(t) + \boxed{H.O.T.}$$ ignored

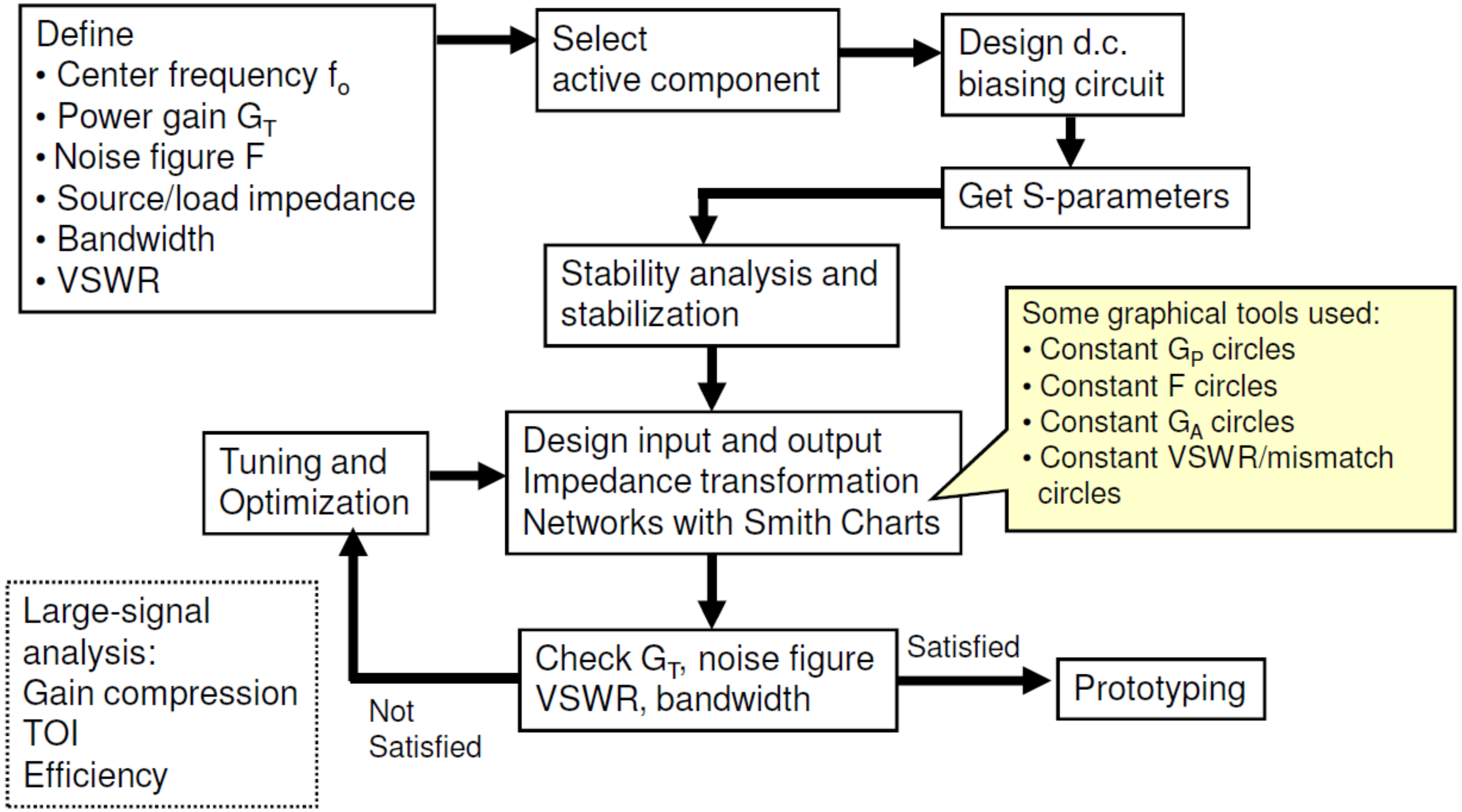


More will be said about this later in large signal amplifier design

These are unwanted components, caused by the term $\alpha_3 v_i^3(t)$, which falls in the operating bandwidth of the amplifier.

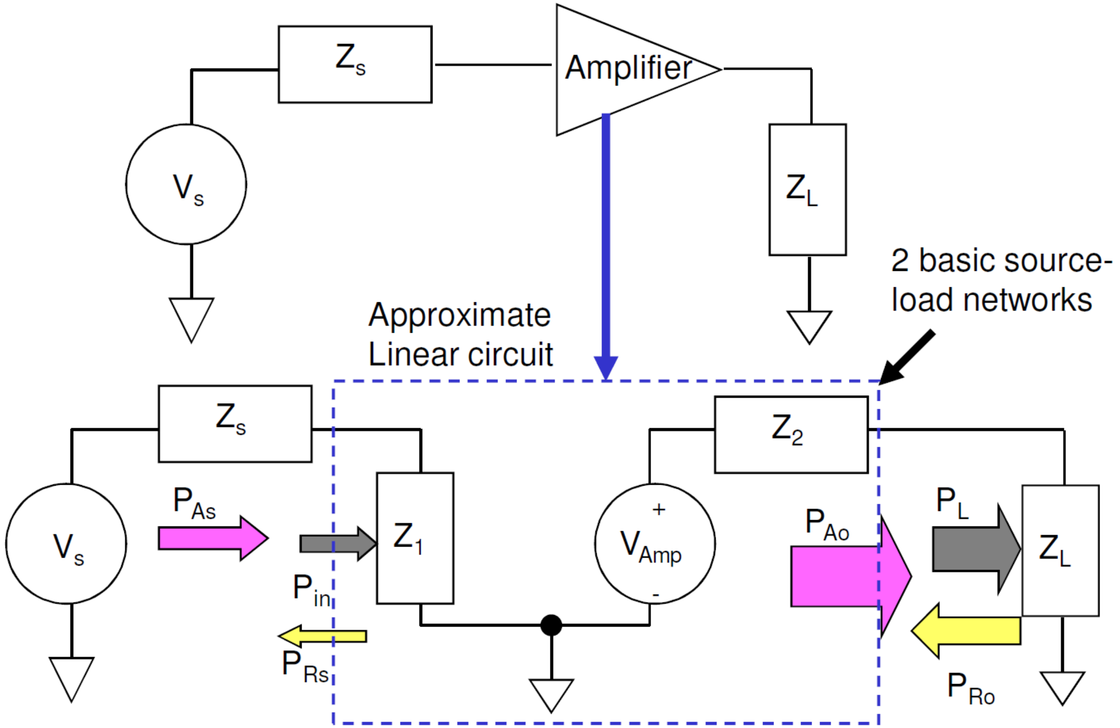
Circuit Design (Amplifier)

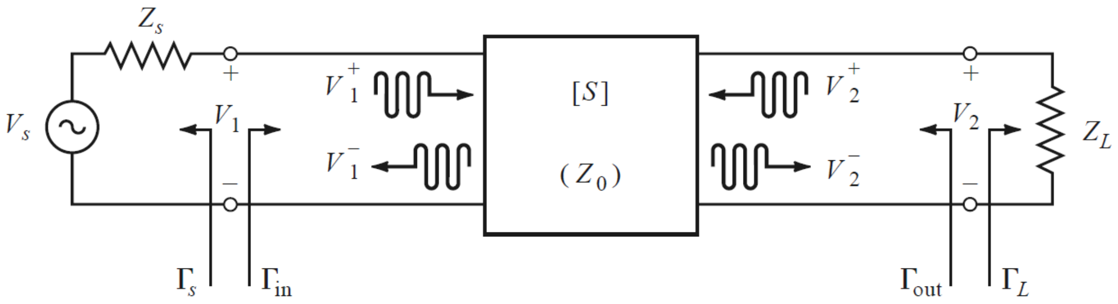
Small Signal Amplifier Design Flow



Circuit Design (Amplifier)

Two-port network analysis





Power Gain $G_p = \frac{\text{Power delivered to load}}{\text{Input power to Amp.}} = \frac{P_L}{P_{in}}$

Available Power Gain $G_A = \frac{\text{Available load Power}}{\text{Available Input power}} = \frac{P_{Ao}}{P_{As}}$

Transducer Gain $G_T = \frac{\text{Power delivered to load}}{\text{Available Input power}} = \frac{P_L}{P_{As}}$

The effective power gain

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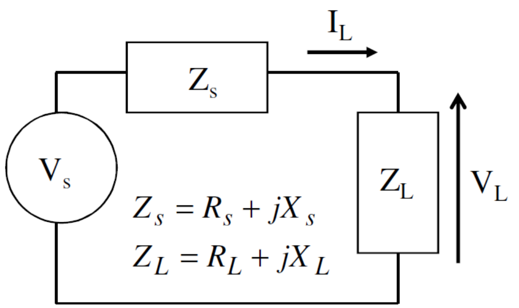
Circuit Design (Amplifier)

Conjugate Matching: theory of maximum power transfer



Basic source-load network

Time averaged power dissipated across load Z_L: $P_L = \frac{1}{2}\mathrm{Re}\{V_L I_L^*\}$

where $V_L = \frac{V_s Z_L}{Z_s + Z_L}$ $\quad I_L = \frac{V_s}{Z_s + Z_L}$

$$P_L = \frac{1}{2}\mathrm{Re}\left\{\frac{V_s Z_L}{Z_s+Z_L}\cdot\left(\frac{V_s}{Z_s+Z_L}\right)^*\right\} = \frac{1}{2}\mathrm{Re}\left\{\frac{|V_s|^2 Z_L}{|Z_s+Z_L|^2}\right\}$$

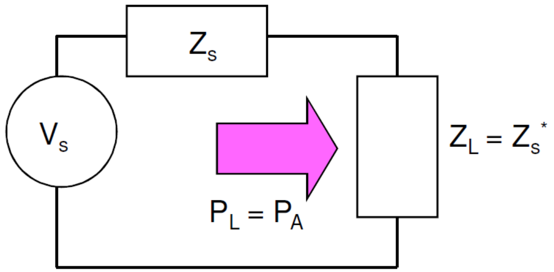
$$\Rightarrow P_L = \frac{1}{2}\frac{|V_s|^2 R_L}{(R_s+R_L)^2+(X_s+X_L)^2}$$

$$P_L = P_L(R_L, X_L)$$

Letting $\frac{\partial P_L}{\partial R_L} = \frac{\partial P_L}{\partial X_L} = 0$

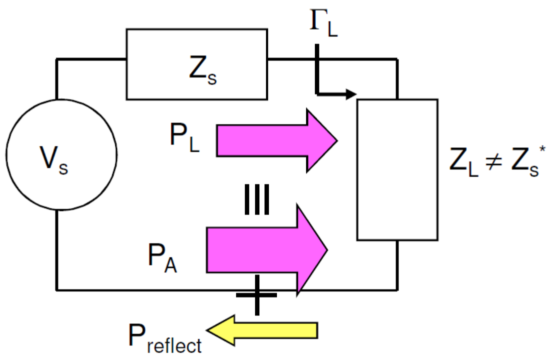
We find that the value for R_L and X_L that would maximize P_L is
$R_L = R_s$, $X_L = -X_s$.
In other words: $Z_L = Z_s^*$

To maximize power transfer to the load impedance, Z_L must be the complex conjugate of Z_s, a notion known as Conjugate Matched.



Under conjugate match condition:

$$P_{L(\max)} = \frac{|V_S|^2}{8R_S} = P_A$$ ← Available Power



Under non-conjugate match condition:

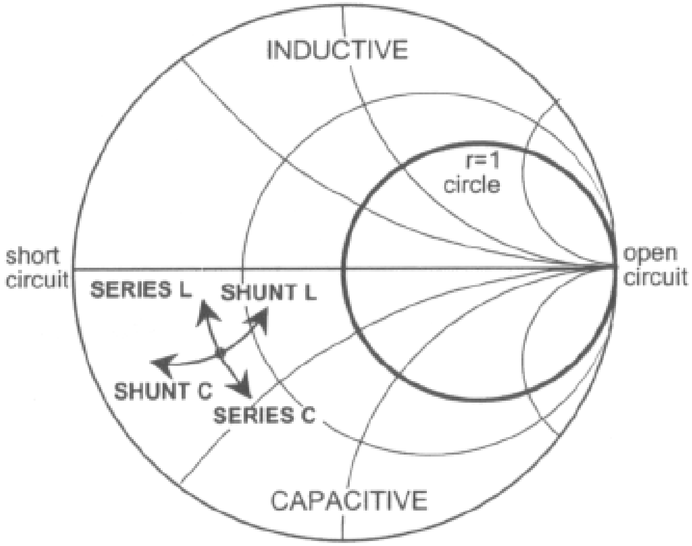
$$P_L < \frac{|V_S|^2}{8R_S} = P_A - P_{Reflect}$$

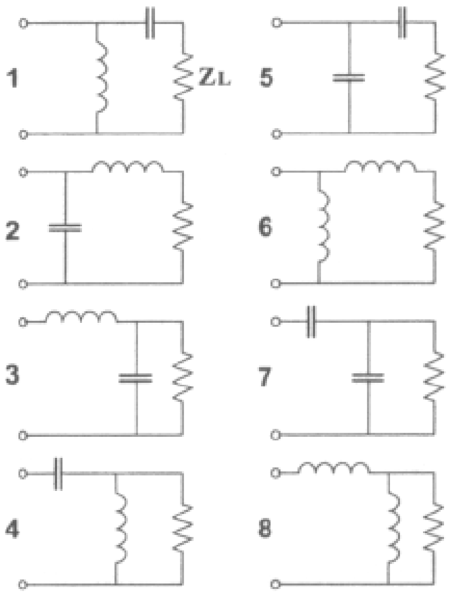
or $P_L = P_A\left(1-|\Gamma_L|^2\right)$

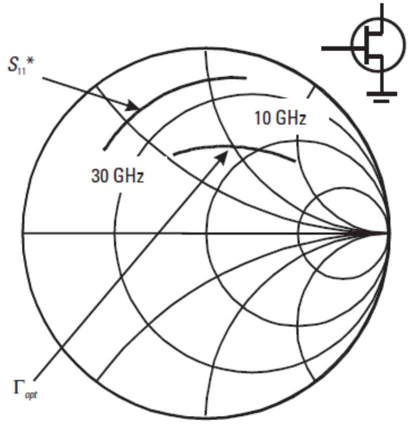
We can consider the load power P_L to consist of the available power P_A minus the reflected power $P_{reflect}$.

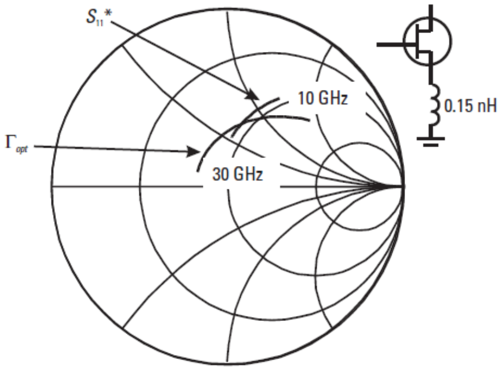
Circuit Design (Amplifier)

I/O matching and series feedback



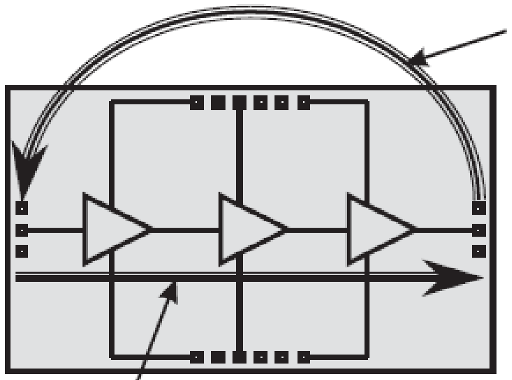






Circuit Design (Amplifier)

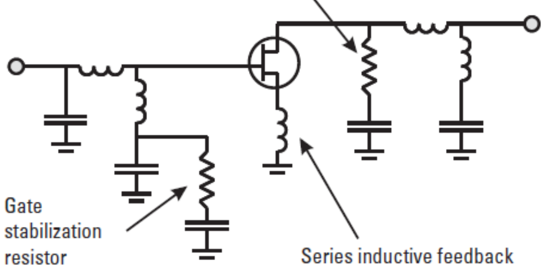
Stability design

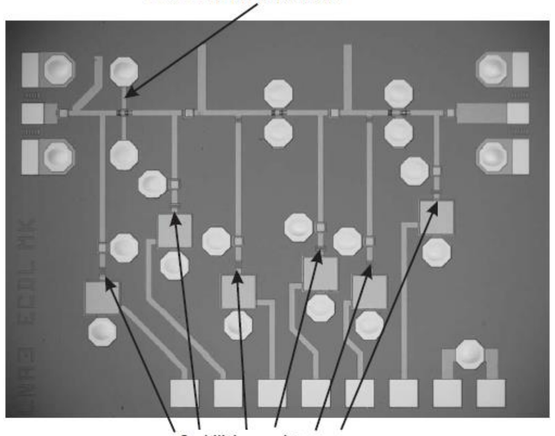


$G < B$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

- Gain < Backward isolation;
- Single-stage gain < 10dB.





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Circuit Design (Amplifier)

Example:

- Frequency：2～2.5GHz
- Noise Figure：<1dB
- Gain：>20dB
- Power
- consumption：5V/55mA
- P-1：>10dbm

Process	PH25 Low Noise	PH15 Low Noise	PPH25 Power	PPH15 Power	HB20P Power	HP07 Power	BES
Active device	pHEMT	pHEMT	pHEMT	pHEMT	HBT	MESFET	Schottky
Power Density	250 mW/mm	300 mW/mm	700 mW/mm	600 mW/mm	3500 mW/mm	400mW/mm	
Gate Length	0.25 µm	0.15 µm	0.25 µm	0.15 µm	2 µm Emitter width	0.7 µm	1 µm
I_{DS} (gm max) $I_{DS\ SAT}$/I_CHBT	200 mA/mm 500 mA/mm	220 mA/mm 550 mA/mm	200 mA/mm 500 mA/mm	300 mA/mm 600 mA/mm	0.3 mA/µm²	300 mA/mm 450 mA/mm	
V_{BDS} / V_{BCE}	> 6V	> 4.5V	> 12V	> 8V	> 16V	> 14V	< -5V (Anode/ Cathode
Cut off freq.	90 GHz	110 GHz	50 GHz	75 GHz	25 GHz	15 GHz	3 THz
Vpinch	- 0.8 V	- 0.7 V	- 0.9 V	- 0.9 V	-	- 4.0 V	-
Gm max/ β	560 mS/mm	640 mS/mm	450 mS/mm	550 mS/mm	70	110 mS/mm	
Noise / Gain	0.6dB / 13dB @10GHz 2dB / 8dB @40GHz	0.5dB / 14dB @10GHz 1.9dB / 6dB @60GHz	0.6dB/12dB @10GHz	1.6dB/7dB @40GHz	-	-	-

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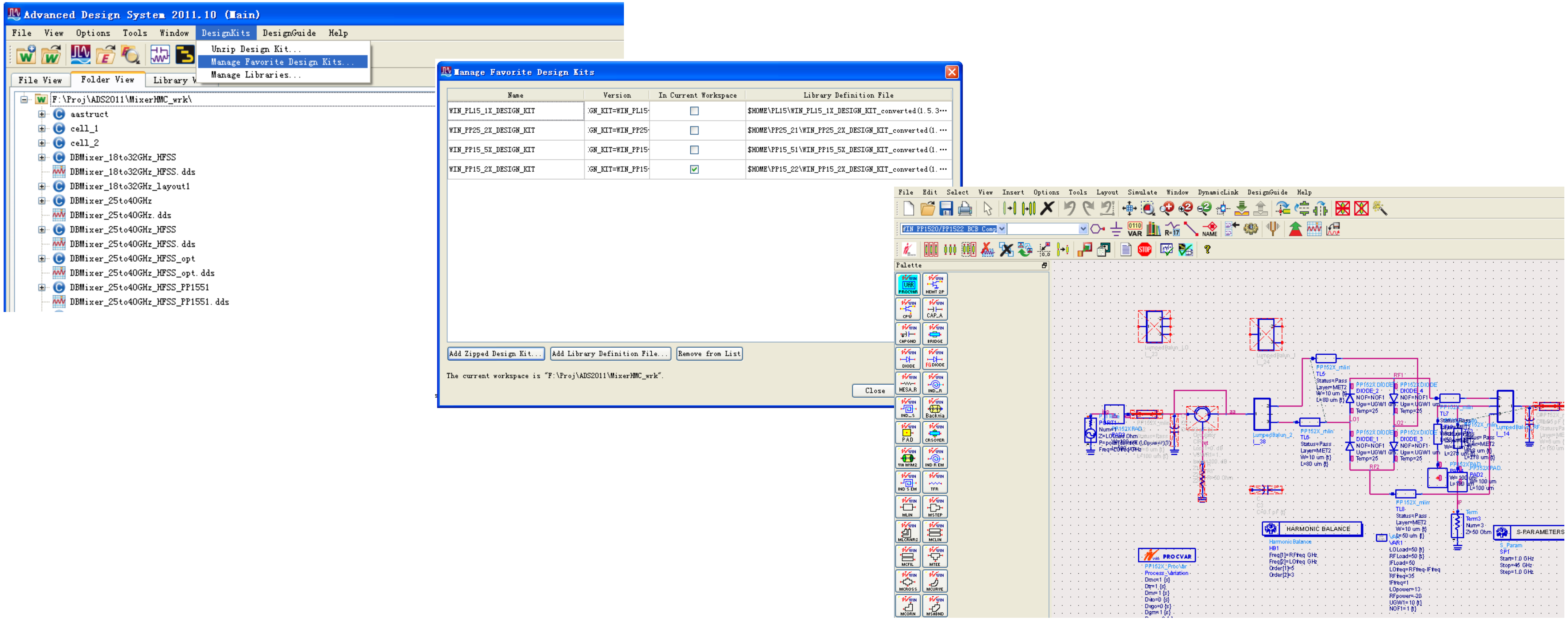
■ Circuit Design (Amplifier)

Example:



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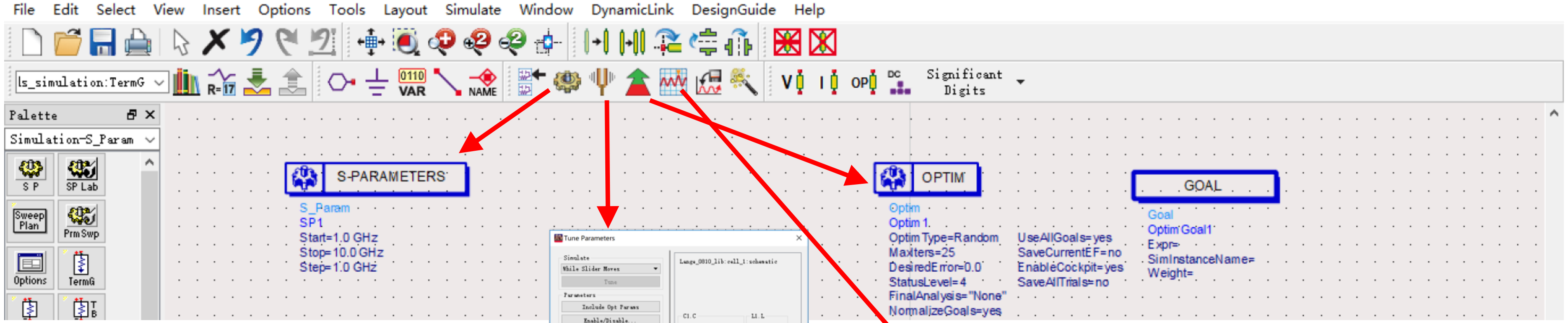
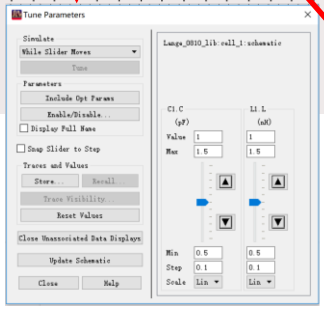
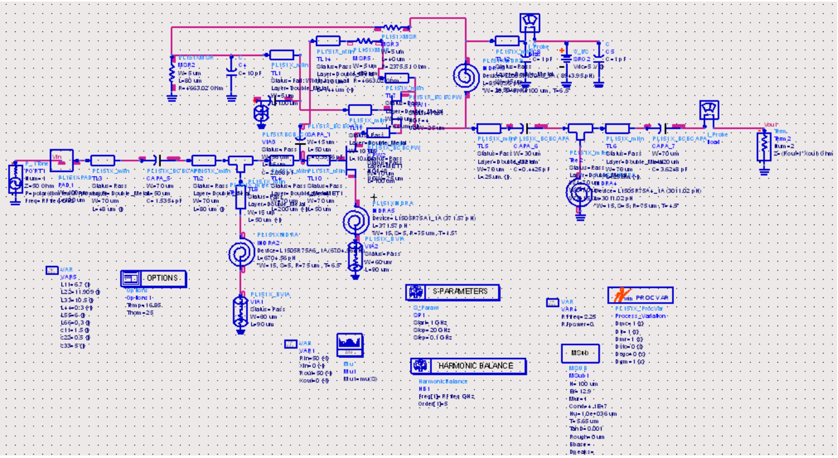
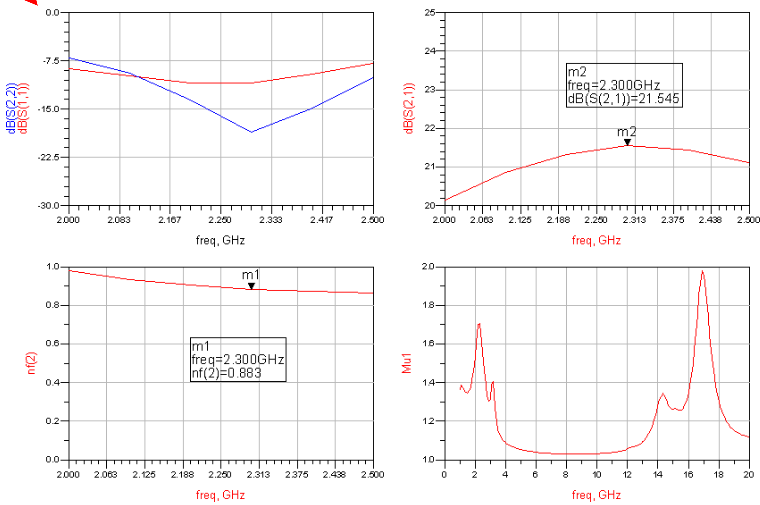
Circuit Design (Amplifier)

Example:



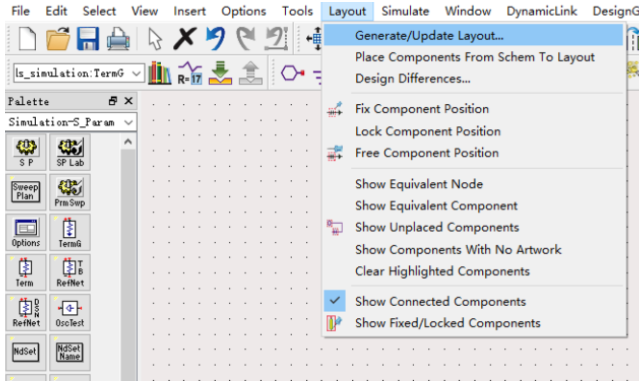


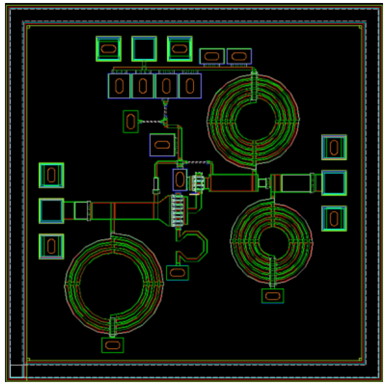




■ Circuit Design (Amplifier)

Example:



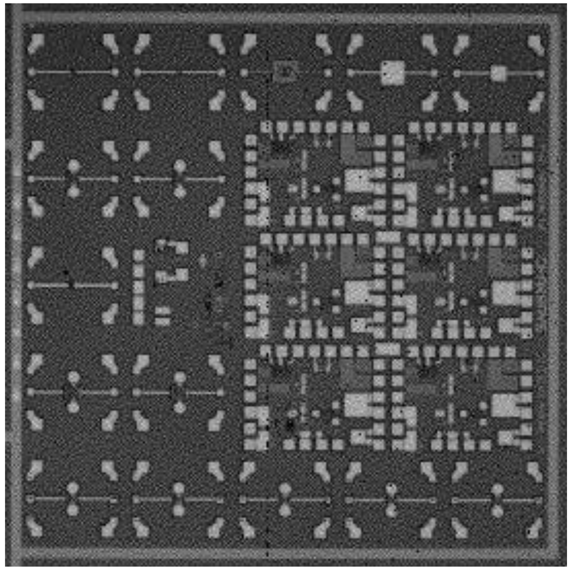


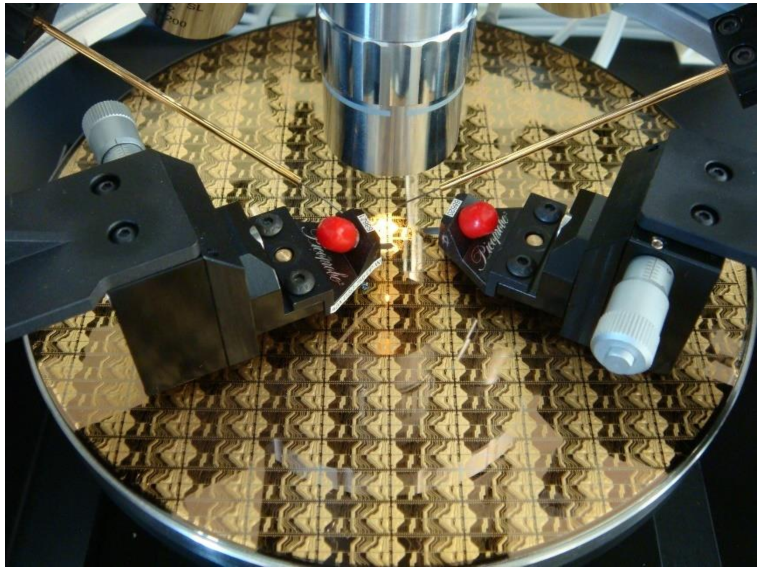
Generate layout

Layout & GDS file

Foundry service

PCM and RFOW

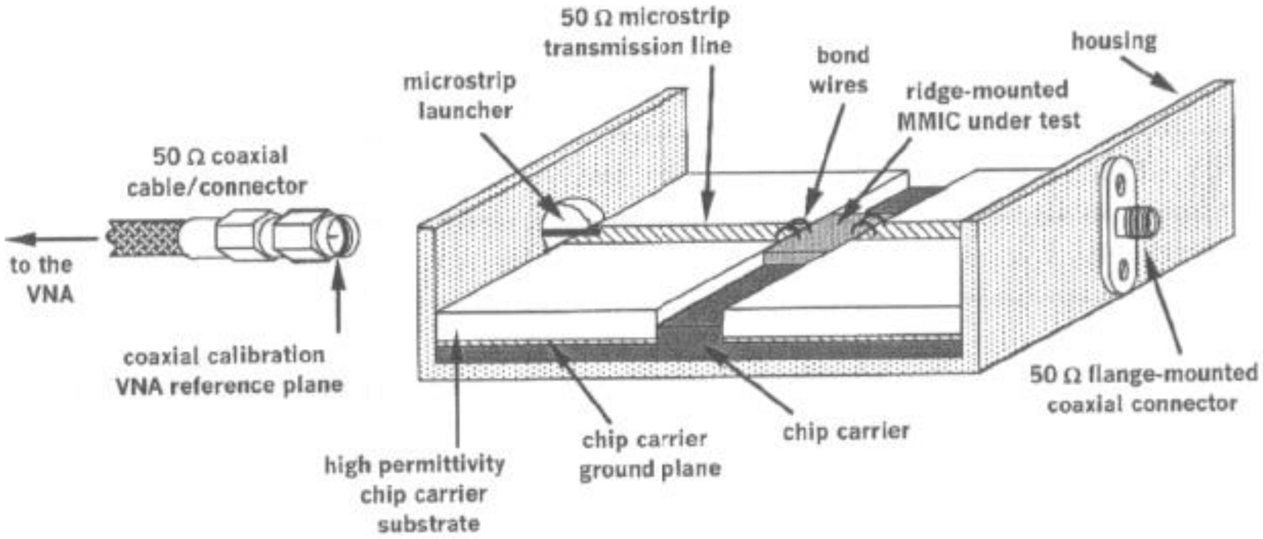


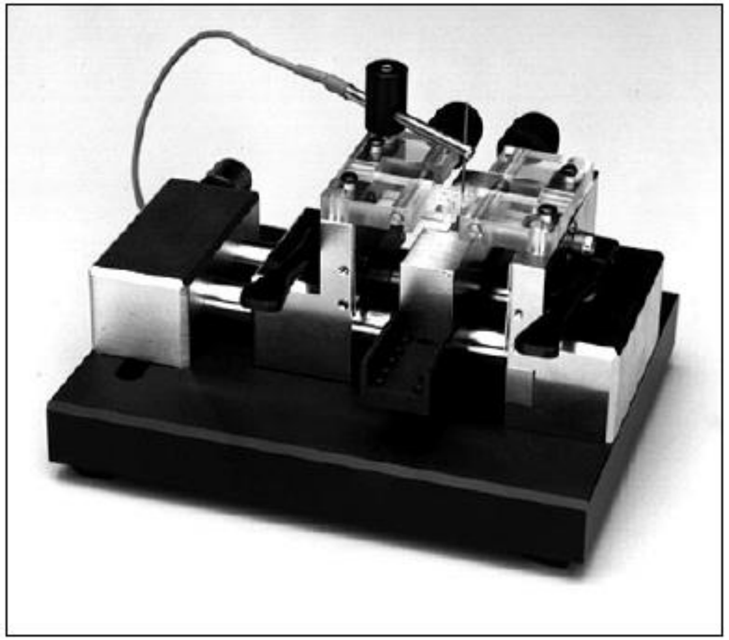


Process Control Monitoring (PCM)

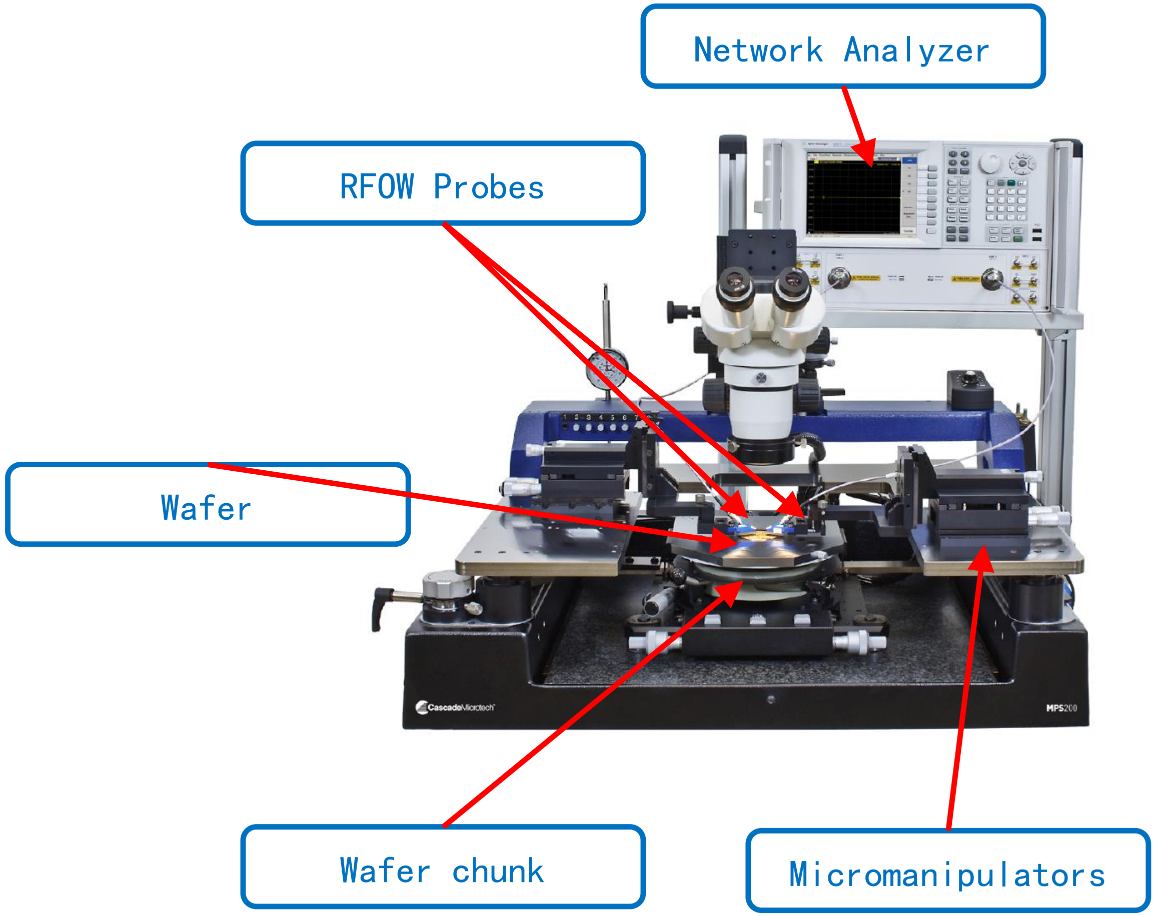
RF On-Wafer Measurement (RFOW)

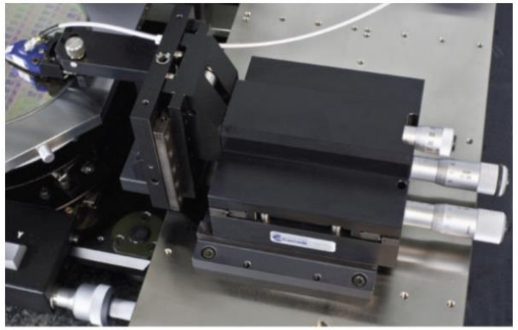
Early On-Wafer-Measurement

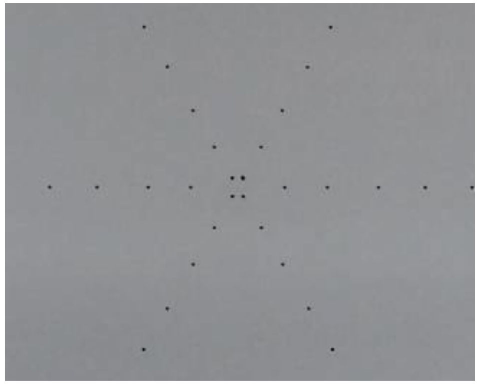




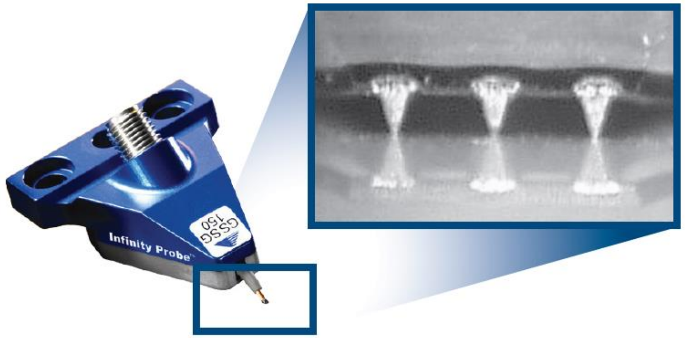
Probe Station

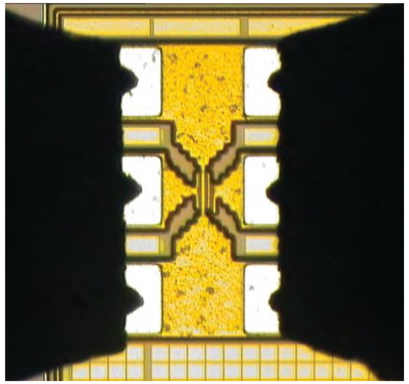


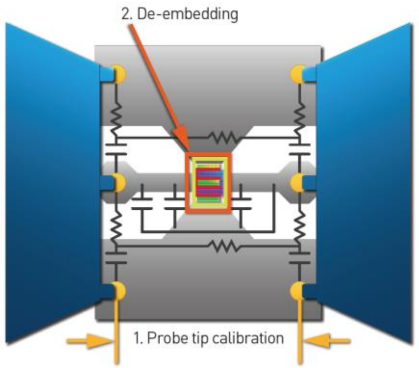


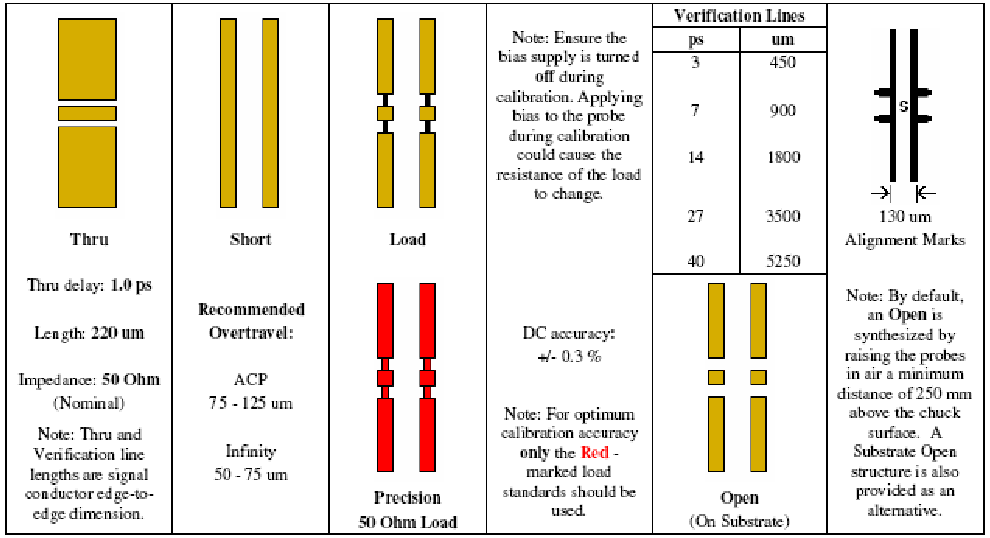


Probe and Calibration

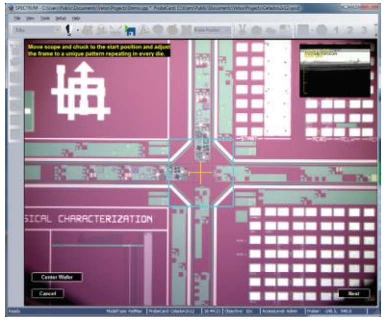




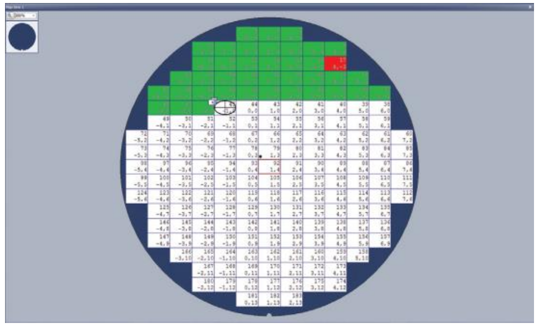




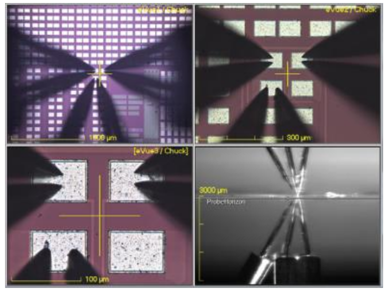
Automatic Measurement



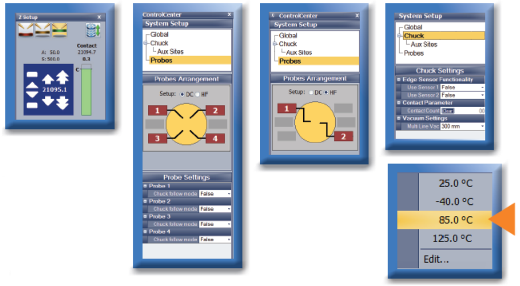
Alignment Tools



Test Cycle Automation



Probe Placement



Visual Reference Points

References

- Steve Marsh: **Practical MMIC Design**, Artech House, 2006.
- Jean-Luc Gautier: **Design of Microwave Active Devices**, ISTE Ltd., 2014.
- Leo G. Maloratsky: **Integrated Microwave Front-Ends with Avionics Applications**, Artech House, 2012.